International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 1, Issue 3, December 2014)

Implementation of Space Time Block Coded (STBC) Multiple Input Multiple Output encoder and decoder on FPGA using VHDL

Mr. R.Sai Shravan
Pursuing M.Tech scholar, VLSI-System Design
Aurora's Scientific, Technological and Research Academy
Hyderabad, Telangana, India
Shravansai27@gmail.com

Mrs. A.Triveni
Lab Faculty, Dept.of E.C.E
Aurora's Scientific, Technological and Research Academy
Hyderabad, Telangana, India

Mrs. D.Kavitha
Associate Professor, Dept.of E.C.E
Aurora's Scientific, Technological and Research Academy
Hyderabad, Telangana, India

***Abstract*— In this paper presents a simple two-branch transmit diversity system, using two transmit antennas and two receive antenna the scheme provides the same diversity order as maximal-ratio receiver combining (MRRC) with one transmit antenna, and two receive antennas. In this system each channel uses multiple input multiple output Alamouti space time block codes over Rayleigh flat hazy channels. The entire a computationally adequate program is carried out on applications based on FPGA. The decoding algorithm and other communication blocks are realized by using VHDL programming language. The STBC decoder will also be realized which generates the required appropriate codes from encoder to validate the entire design cycle.**

Index Terms*—Component *STBC Encoder, Channel modeling, ML Detector, STBC Decoder, BPSK* Introduction *(Heading 1)

I. INTRODUCTION

In wireless communications systems, multiple-input and multiple-output is the use of multiple antennas at both the transmitter and receiver to develop communication performance more. It is a one part of several forms of smart antenna technologies used. The terms input and output does denotes the input and output of the system carrying signal but not the having different antennas. Multiple Input Multiple Output (MIMO technology has drawn consideration in communication systems because it offers significant increases in data throughput and link range without additional transmit power or bandwidth. Thus it achieves this by higher spectral efficiency (more bits per second per hertz of bandwidth) and link reliability or diversity (reduced fading).[1]

A. Multi-user types:

Recently, the research on multi-user MIMO technology has been emerging. While full multi-user MIMO (or network MIMO) can have higher potentials, from its practicality the research on (partial) multi-user MIMO (or multi-user and multi-antenna MIMO) technology is more active.

B. Multi-user MIMO (MU-MIMO)

MU-MIMO is being treated as one of candidate technologies adoptable in the specifications such as wimax and 3GPP standards. Since MU-MIMO is more feasible to low complexity mobiles with small number of reception antennas than SU-MIMO with the high system throughput capability.

The MIMO refer to Multi-Input-Multi-Output (MIMO) , here we use 2x2 MIMO system. One possible way to improve the reliability of wireless communications is to employ diversity. Diversity is the technique of transmitting the same information across multiple channels to achieve higher reliability.

C. Space time block coding (STBC):

It is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-relocation.
In a general form, an STBC can be seen as a mapping of nN complex symbols {s1, s2, · · ·, sN } onto a matrix S of dimension nt × N:

$$\{s1, s2, \cdots, sN\} \rightarrow S$$

An STBC code matrix S taking on the following form:

$$\mathbf{S} = \sum_{n=1}^{n_N} (\bar{s}_n \mathbf{A}_n + j\tilde{s}_n \mathbf{B}_n),$$

where {s1, s2, · · · , snN} is a set of symbols tobe transmitted with $\bar{s}_n = \mathrm{Re}\{sn\}$ and $\tilde{s}_n = \mathrm{Im}\{sn\}$, and with fixed code

International Journal of Advanced Research Foundation
Website: www.ijarf.com, ISSN: 2394-3394

matrices {An, Bn} of dimension nt × N are called linear STBC.[5]

D. Alamouti Code:

Historically, the Alamouti code is the first STBC that provides full diversity at full data rate for two transmit antennas. A block diagram

of the Alamouti space-time encoder is shown in Fig 1.

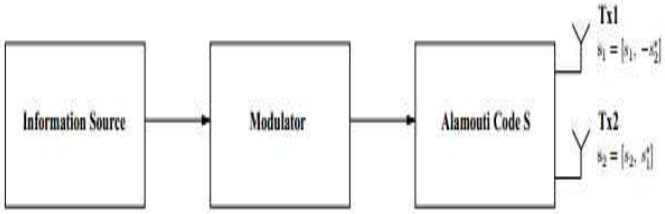

Fig. 1. The block diagram of the Alamouti space-time encoder

The information bits are first modulated using an M-ary modulation technique. The encoder receives the block of two modulated symbols s1 and s2 in each encoding operation and hands it to the transmit antennas according to the code matrix

$$S = \begin{bmatrix} s_1 & s_2 \\ -s_2^* & s_1^* \end{bmatrix} \quad (1)$$

In Eq. 1 the first row represents the first transmission period and the second row the second transmission period. During the first transmission, the symbols s1 and s2 are transmitted simultaneously from antenna one and antenna two respectively. In the second transmission period, the symbol $-s_2^*$ is transmitted from antenna one and the symbol s_1^* from transmit antenna two [4].

So the below sections illustrates the operation of proposed design and implemented in same manner. Section II describes the proposed design. Section III describes about the implementation of the proposed design. Section IV illustrates the results and discussion. Section V illustrates the conclusion of project paper.

II. PROPOSED DESIGN

In the proposed design, STBC transmission blocks are also designed to validate the complete STBC Implementation. Thus, the design consists of STBC Transmitter blocks and Receiver blocks as shown in Fig 2. Transmitter consists of Symbol modulation and STBC Encoder blocks; Receiver consists of noise parameter estimation, STBC decoder and Maximum Likelihood Decoder as the main blocks.

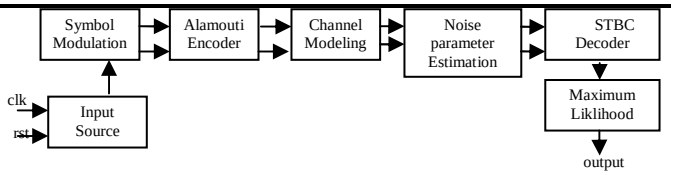

Fig. 2.Block Diagram of the proposed design

In the symbol modulation the inputs from the source is converted into block of codes, these codes are encoded and transmitted from the different antenna at different time intervals then at the receiver point these block codes are received and decoded.

In a classical one-transmitter section, symbols $\boldsymbol{S_0}$, $\boldsymbol{S_1}$, $\boldsymbol{S_2}$, S_3 are transmitted at time intervals t, t+T, t+2T, t+3T respectively. In a two transmitter Alamouti encoder scheme however, the symbols $\boldsymbol{S_0}$ and $\boldsymbol{S_1}$ are transmitted simultaneously from two transmit antennas ***Transmitter*$_1$** and ***Tranmitter*$_2$** respectively, at time interval t. At time interval t+T, ***Transmitter*$_1$** transmits symbol $-\boldsymbol{S_1}^*$ and ***Transmitter***$_2$ transmits symbol $\boldsymbol{S_0}^*$.

In the receiver section first S_0 is received at the ***Receiver*$_1$** and S_1 is received at second ***Receiver*$_2$** at a regular time intervals. Next the synbol $-\boldsymbol{S_1}^*$ is transmitted from transmitter1 and is received at the receiver 1 and the symbol $\boldsymbol{S_0}^*$ is received at the receiver 2. The symbol which are transmitted and received is effected by some noise, the noise of the signal is estimated at the noise parameter estimation section. Later the Signal or symbol is decode dat the STBC decoder section. The decoded signals contains the noise parameters that are not necessary, so the maximum liklihood detector is used to detector the signal which has more strength and complexity. At the final the maximum likli signal which is nearer to the original signal is detected as detected bit which is an final output.

III. A BRIEF OVERVIEW OF PROPOSED DESIGN

A.STBC Transmitter

The STBC transmitter consists of different set of blocks such as clock generator which is used to generate clock signal for the design the inputs of clock generator are rst, master_clk, data_bit and outputs are ant0_out and ant1_out. The data bit is given to symbol mapper that will convert data bit to i_sym and q_sym these output's will be shifted to pipo block so that with the same clock the data is processed to next state, STBC_state is used as a select pin to S block it works as a mux according to select bit the operation will be selected and generates the signals selected_i_sym_ant0 and the other signals are also generated in that manner signal such as selected_i_sym_ant1.

Using the phase_inc_word the phase_acc section generates address to the LUT_cos and lut_sin, LUT_cos and lut_sin generates the amplitude according to address amplitude

International Journal of Advanced Research Foundation
Website: www.ijarf.com, ISSN: 2394-3394

signals will be supplied to the multiplier blocks for further process. Frame clk is used to generate the enable signals to the multiplier section this is shown in below figure 3.

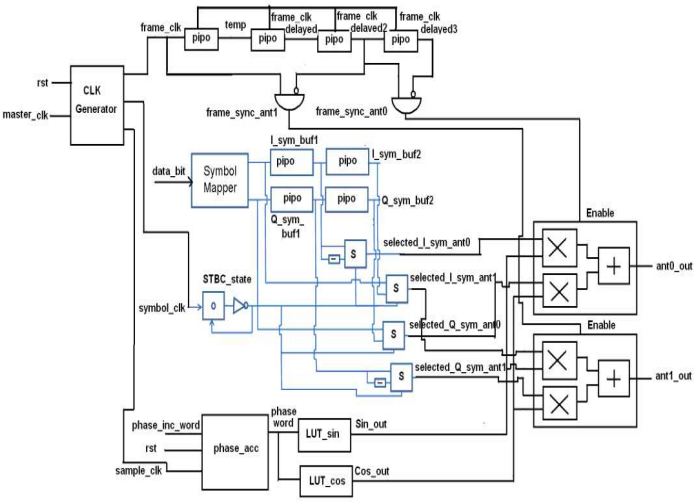

Fig. 3. Block diagram of STBC transmitter

B. Implementation block diagram

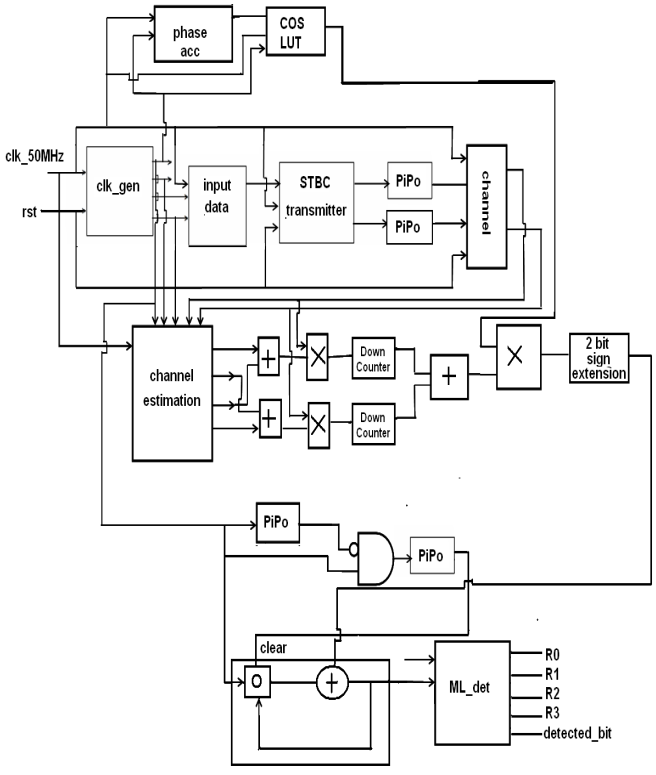

Fig. 4. STBC top module block diagram

The above shown figure is an top module block diagram which consists of different blocks such as clock generator, input data generator, maximum liklihood detector, channel estimator and channel module. The process of signal generation and transmission is whole carried out at the transmission part and receiver section the channel estimation.

The inputs to the input data generation module is reset, symbol clock and frame clock and the output is data bits. This module consists of 5-bit up counter, ROM. The 5-bit up counter increments by one bit when the frame sync is 0 and the symbol clock is 1 and this incremented value will be given to the ROM to read as address and the ROM gives the data bits as output. This data bits are given as input the transmitter. The output from channel estimation is the input for combiner and the maximum likelihood detector. From the ML detector detects the signal which has less noise. The register transfer level schematic for top module is shown in the results and discussion section.

IV. RESULTS AND DISCUSSION

Register Transfer Level (RTL) schematic for the complete logic is given in the Fig 5.

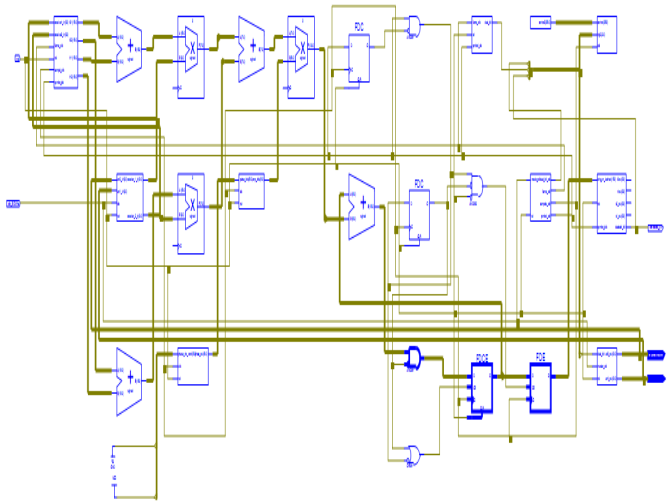

Fig. 5.Register Transfer Level schematic of the complete design

Simulation results of the proposed design are given in the Fig 6 below. The 1st waveform is the main clock used in the complete logic. The 2nd waveform shows input data bits come from input data generator module, the next two waveforms are inputs of transmitter cos and sin waveforms inputs transmitted through transmitter. The next wave form is the main input i.e., data_bit wave after that remaining four waveforms are the channel parameter estimator waveforms. The next of the parameter waveforms are the noise waves which are added. The last waveform is the final detected output from the Maximum Likelihood Detector which is the output of complete design.

The inputs of the transmitter are the analog signals. The results are shown in below Fig 6.

International Journal of Advanced Research Foundation
Website: www.ijarf.com, ISSN: 2394-3394

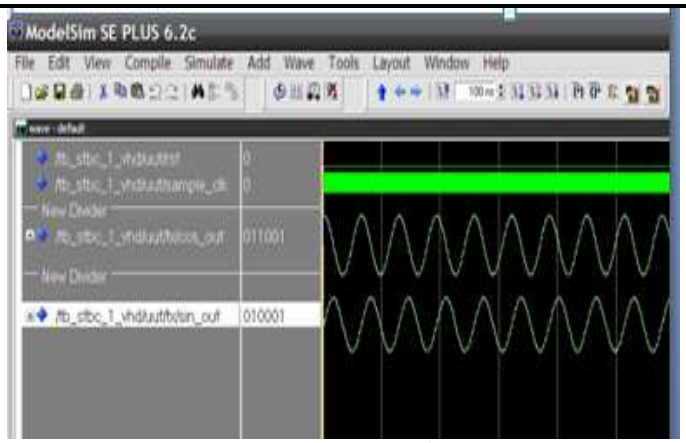

Fig. 6. Cos and sin input waveforms

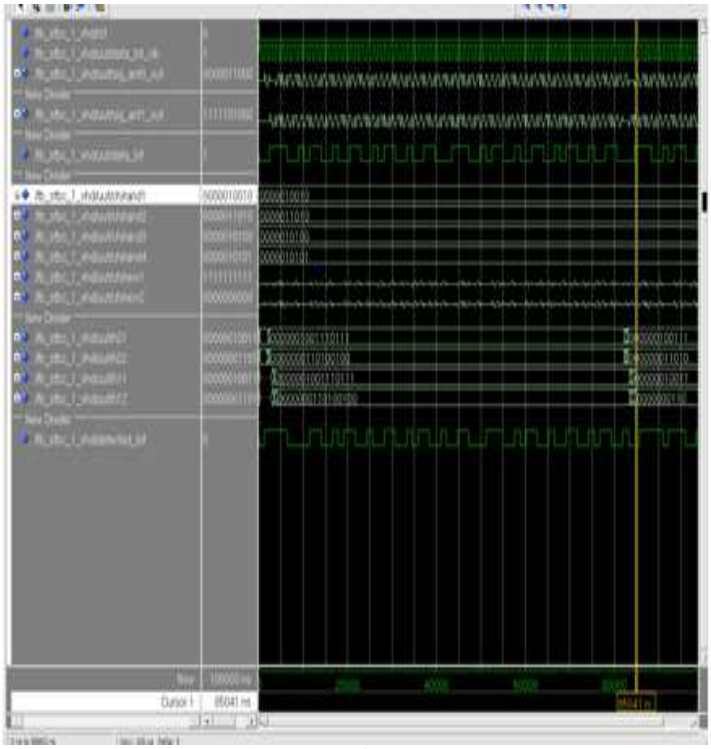
Fig. 7.Simulation results of the complete design

V. CONCLUSIONS

In this project Alamouti STBC transmitter is shown to be in upper bound for transmitting data through communication channel with respect to combating fading and communication loss. The STBC encoding allows us to get Space wise (by multi transmitting antennas) and Time wise (corresponding to different transmitting times) encoding of blocks of data to be transmitted by which reliability of data transmission is provided. At the receiver part, ML Decoder gives the reliable data by collecting channel estimated parameters and received signals. In MIMO with STBC when selecting the number of transmit/receive antennas, several practical considerations must be taken into account as under strict delay constraints, achieving high diversity gains (i.e. high reliability) becomes critical in order to minimize the need for retransmissions. Since transmit/receive diversity gains experience diminishing returns as their numbers increase, complexity considerations dictate the use of small antenna arrays (typically no more than 4 antennas at each end).

REFERENCES

[1] G. Foschini, "Layered space-time architecture for wireless communication in a fading environment when using multiple antennas," Bell Lb. Techn. 1. vol. I, no. 2, pp. 4159, 1996.
[2] P. Green and D. Taylor, "Smart antenna software radio test system," Proceedings of the First IEEE International Work-shop on Electronic Design, Test and Applications.,vol.1,pp. 68–72, Jan. 2002.
[3] "Experimental verification of space-time algorithms using the smart antenna software radio test system (sasrats) platform," Personal, Indoor and Mobile Radio Communications, 2004. PIMRC 2004. 15th IEEE International Symposium on, vol. 4, pp. 2539–2544, 2004.
[4] "Implementation of a high speed four transmitter space-time encoder using field programmable gate array and parallel digital signal processors," Proceedings of the Third IEEE International Workshop on Electronic Design, Test and Applications., pp. 466–471, Jan. 2006.
[5] S. Alamouti, "Space block coding: A simple transmitter diversity technique for wireless communications," IEEE J. Select. Areas. Communication, vol. 16, pp. 1451–1458, Oct. 1998.
[6] D. Gesbert et al., "From theory to practice: An overview of mimo space-time coded wireless systems," IEEE Journal on Selected Areas in Communications, vol. 21, pp. 281–302, Apr. 2003.

About the authors:

Mr. R.Sai Shravan[1] received B.Tech degree in ECE from JNTUH in 2012, pursuing M.Tech (2012-2014) in the stream of VLSI-System Design at Aurora's Scientific, Technological and Research Academy, (Affiliated to JNTUH) Hyderabad.

Mrs. A.Triveni[2] received M.Tech degree in VLSI from JNTUH, B.Tech degree in ECE from JNTUH 2002, presently working as Lab faculty in ASTRA, Hyderabad.

Mrs. D.kavitha[3] received M.Tech degree in VLSI from JNTUH in 2010, B.E degree in ECE from OU in 2003, Diploma in ECE from SBTET in 1998. Presently working as Associate professor in ASTRA, Hyderabad.