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Design and Implementation of TSPC and E-TSPC based Low Power Single Phase Clock Distribution in SOC Technology

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***Abstract*- The clock distribution network synchronizes the flow of data signal between data path. One of the important functional blocks in frequency synthesizer is the high speed dual module prescaler. Normally for a multi clock domain network we develop a multiple PLL to cater the need, this project aim for developing will supply for the multi clock domain network. A voltage controlled differential injection locked frequency divider (VCDILFD) is used as the first frequency divider in the PLL feedback to reduce power consumption and eliminate the need for an off chip frequency divider. We have performed proposed wideband E-TSPC prescaler simulation cadence virtuoso 180nm technology and simulations have been compared for multiple VDD. Verilog programming of multi-modulus prescaler is in CAD IUS (incisive unified simulator). The low power synthesis is done in cadence RTL (register transfer level) and the design is implemented in cadence encounter SOC by using Library Exchange Format (LEF) file of proposed wideband E-TSPC. This project is highly useful and recommended for communication applications like Zigbee, Bluetooth, WLAN frequency synthesizers are proposed based on pulse-swallow topology and the design of the design goes from cell based design to system on chip technology in cadence EDA tools.**

***Keywords* - Frequency synthesizer, E-TSPC, VCDILFD, Prescaler, Dynamic logic, LEF, PLL, RTL, IUS, EDA.**

1. INTRODUCTION

The demand for lower power, and multiband RF circuits increased in conjunction which need of higher level of integration. The frequency synthesizer is mainly implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first stage frequency divider consumes a large portion of power in frequency synthesizer. The synthesizers for WLAN applications at 5 GHz consume up to 25mW in CMOS, where the first-stage divider is implemented using an voltage controlled differential injection-locked divider which consumes large chip area and has a narrow locking range. The frequency synthesizer at 6 GHz consumes 9.7mW 1.8 V supply, where its complete divider is implemented using the source-coupled logic (SCL) circuit which allows higher operating frequencies but uses more power. Dynamic flip-flop are faster and consume less power compared to static dividers. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the clock skew and jitter problem the adoption of single-phase clock latches in frequency dividers has been limited clock to PLL with applications below 5GHz[7] [8]. The frequency synthesizer uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.15 mW. Most frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizer. In this paper a Dynamic logic multiband flexible integer-n divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multi modulus 32/33/47/48/64/66/94/96 prescaler as show in fig1. The divider also used an improved low power loadable bit-cell for the Swallow S-counter.

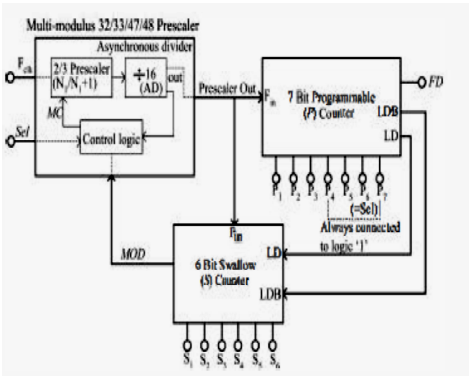

Fig.1. Proposed dynamic logic multiband flexible Divider.

II. DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuit are the propagation delay and power consumption of the maximum operating frequency of a digital circuit is calculated is given by

$$\mathbf{Fmax = 1/tpLH + pHL} \qquad \mathbf{(1)}$$

It is the tpLH and tpHL are the propagation delays of the low-to-high and high-to-low of the gates, respectively.
The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is a linearly proportional to the operating

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frequency is given by the sum of switching power at each output node as in equation (2)

$$\textbf{Pswitching} = \sum_{k=1}^{n} fclk\ CLk\ \mathrm{v}^2 \boldsymbol{dd} \qquad (\mathbf{2})$$

Where $n\ is$ the number of switching nodes, fclk is the clock frequency, CLk is the load capacitance at the output node of the kth stage, and vdd is the supply voltage. the short circuit power occurs in dynamic circuits. When there exists a direct path from the supply to ground which is given by

$$Psc = Isc * Vdd \qquad (3)$$

Where Isc is the short-circuit current. The analysis in E-TSPC show that in power is much higher in the E-TSPC circuits has the of higher operating frequency than that of the TSPC circuit due to the E-TSPC reduction in load capacitance, but it consumes more power than the TSPC circuits does for a given transistor size. The following is based on the latest design using the popular 0.18u CMOS process.

III. WIDEBAND E-TSPC 2/3 PRESCALER

The circuit which divides the frequency of the input signal by either 2/3, depending on the logic state of the modulus control signals MC. ETSPC design removes the transistor stacked structure so that all the transistors are free of the body effect. ETSPC is used for this low power and high frequency applications. The wideband single phase clock 2/3 prescaler used in design does not consist of two D-flip-flop and two NOR gates embedded in the flip-flops as in Fig 2b.

The first NOR gate is embedded in the last stage of DFF11 and the 2^{nd} NOR gate is embedded in the first stage of DFF21.here, the transistors M2, M25, M4 and M8 in DFF11 helps to eliminate the short circuit power during the modulus divide-by-2 operation. The switching of division ratio between 2 and 3 are controlled by logic signal module control (MC). The load capacitance of wide band prescaler is given by

$$CL - wideband = CdbM19 + 2CgdM19 + CdbM21 + 2CgdM21 + CGM1 \qquad (4)$$

When MC switches from "0"1" transistors M2, M4,M25 and M8 in DFF11 turns off and nodes S1,S2&S3 are switch to logic "0".Since node S3 is "0" and the other input to the NOR gate embedded in DFF21 is Qb the wideband prescaler operates at the divide-by-2 mode. As the removing the switching power contribution of DFF11, since one of the Where CLm is the load capacitance at the output node of the mth stage of DFF21 and Psc1 and Psc2 are the short circuit power in the $2^{nd}$and 3^{rd}stages of DFF21. When the logic signal modulus control (MC) switches from 1 to 0 the logic value at the input of DFF11 is transferred to the input of DFF21 as one of the input of the NOR gate embedded in DFF11 is "0". The wideband prescaler operation at the divide-by-3 mode during the divide-by-2 operation only DFF21 actively participates in the operation and contributes to the total power consumption. Since all the switching activates are blocked in DFF11. Thus the wideband E-TSPC 2/3 prescaler has benefit of saving more than 49% of power during the divide-by-2 operation. The wideband 2/3 prescaler has maximum operating frequency of 6GHZ.

transistor is always OFF in each stage of DFF11, the short circuit power in DFF11 and the first stage of DFF21 is negligible.

The total power consumption of the wideband E-TSPC prescaler in the divide by 2 mode is equal to the switching power and the short circuit power in 2^{nd} and 3^{rd}stages of DFF21 and is given by

$$Pwideband\ divide = \mathrm{fclk\ CLk\ v^2dd} + Psc1 + Psc2 \qquad (5)$$

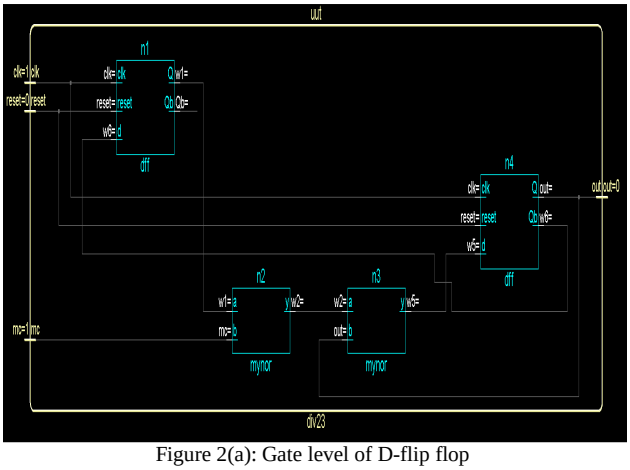

Figure 2(a): Gate level of D-flip flop

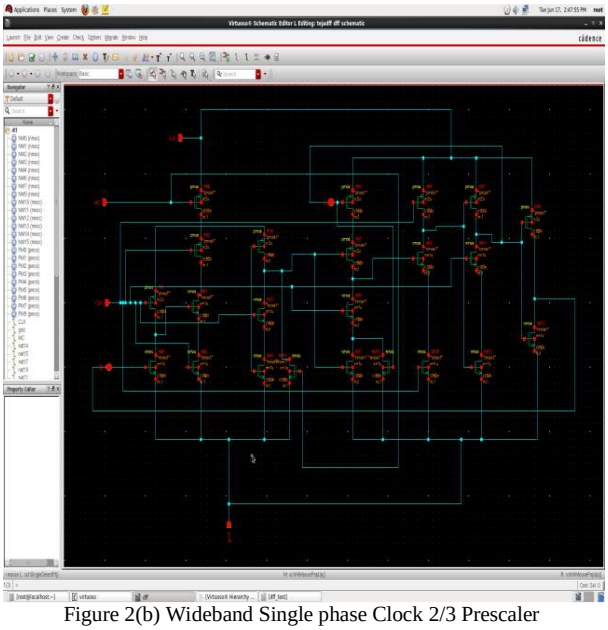
Figure 2(b) Wideband Single phase Clock 2/3 Prescaler

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IV. MULTIMODULUS 32/33/47/48/64/66/94/96 PRESCALER

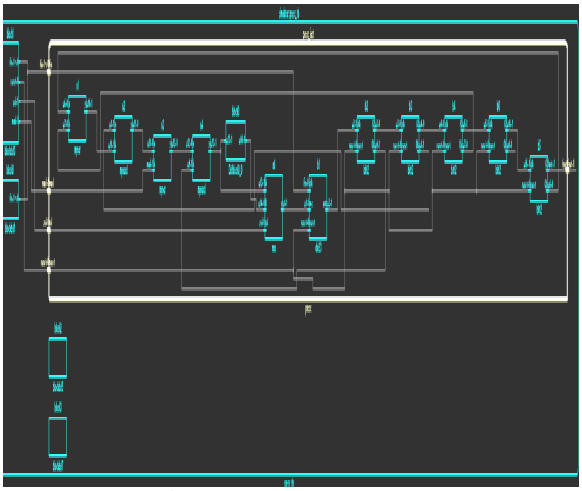

Fig.3. Block diagram of proposed multi-module's 32/33/47/48/64/66/94/96 prescaler.

A multi-modulus prescaler will be used in a fractional-N synthesizer. By cascading or connecting to two or more dual modulus prescalers one can obtain a multi-modulus prescaler and the process is done in cadences EDA tools. The proposed wideband multi-modulus prescaler which can divide the input frequency by 32/33/ 47/48/64/66/94 and 96 is shown in fig.3.

It is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed wideband prescaler performs Additional divisions (divide by 47, 48, 64, 66, 94 and divide by 96) without any extra flip-flops, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multi modulus prescaler consists of the wideband 2/3(N1/(N1+1)) prescaler, four asynchronous TSPC divide-by-2 circuits((AD= 32) and combinational logic circuits to achieve the multiple division ratios beside the usual MOD signal for controlling N/(N+1) divisions, the additional control signal SEL is used to switch the prescaler between 32/33/47/48 and 64/66/94/96 modes.

1) Case 1:SEL='1'

When SEL='1',the output from the NAND2 gate is directly transferred to the input of proposed 2/3 prescaler and the multi modulus operates as the normal 32/64 prescaler, where the division ratio is controlled by the logic signal MOD if MC (modulus control)=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC(modulus control)=0,the 2/3 prescaler operates in the divide-by-3 mode for entering operation. if MOD=1,the NAND2 gate output switches to logic "1"(modulus control, MC=1) output switches to logic "1"(modulus control)MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation the division ratio N performed by the multi modulus prescaler is

$$N=(AD)+(0*(N1+1))=32$$

$$N=(AD)*N1+(0*(N1+1)) =64$$

Where N1=2 and AD=32 is fixed for the entire design. if MOD=0, for 30 input clock MC remains at logic "1",where wideband prescaler operates in divide by 2 mode and, for three input clock cycles, MC remains at logic"0" where the wideband prescaler operates in the divide by 3 mode. In the initial state MOD=0, the multi-modulus prescaler selects the divide by N+1 mode.

$$N+1=((AD-1)+(1*(N1))=33$$

$$N+1=(AD)*N1+(1*(N1))=66$$

1) case 2: SEL='0'

When SEL='0', the NAND2 gate is inverted to directly transferred to the input of 2/3 prescaler and the multi-modulus prescalar operate as a 47/48 prescaler where the division ratio is controlled by the logic signal MOD. If modulus control (MC)=1, the 2/3 prescaler operates in divide by 3 mode and when modulus control (MC)=0, 2/3 prescaler operates in divide by 2 mode which is quite opposite to the operation performed when SEL='0' MOD=1,the division ratio N+1 performed by the multi-modulus prescaler is the wideband prescaler operates in the divide by 3 mode for the entire operation given by

$$N+1=((AD)*(N+1)+(0*N1))=48$$

$$N+1=(AD)+1*(N1*N1)+1*(N1*N1)+1*(N+1))=96$$

If MOD=0, the division ratio N performed by the multi-modulus prescaler is

$$N=(AD)+(1*(N1*N1)+(1*(N1*N1))+N1=47$$

$$N=(AD)*N1+(0*(N1))=96$$

IV. MULTIBAND DIVIDER

The variable frequency divider which can divide the input frequency 32/33/47/48/64/66/94/96 prescaler followed by the program and pulse swallow counters. Only one ripple counter is used for both program and pulse swallow counters. The multi band divider consists of the multimodal's 32/33/47/48/64/66/94/96 prescaler, a 7-bit programmable p-counter and a 6 bit swallow s-counter. The control signal SEL decides whether the divider is operating in lower frequency band (2.4 GHZ) or higher band (5-5.825 GHZ).

A. SWALLOW COUNTER

The 6-bit s-counter show in fig.4 consists of six asynchronous loadable bit cells, a NOR embedded DFF and additional logic

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gates to allow it to be programmable from 0 to 31 for low frequency band and 0 to 47 for the high frequency band.

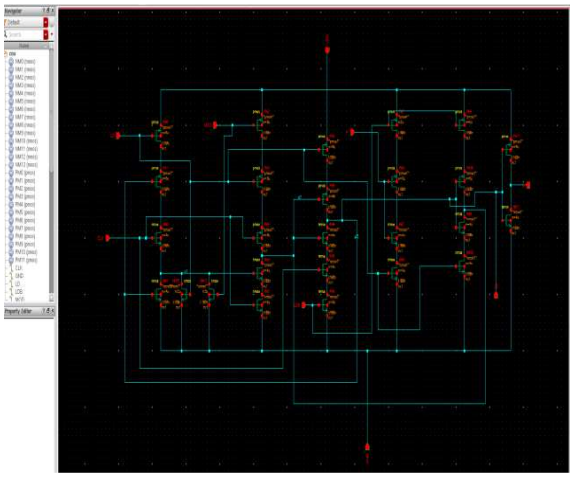

Figure 4: SWALLOW COUNTER

The asynchronous bit cell used in this design is similar to the bit cells except it uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes s1 and programmable, swallow counters start down counting the input clock cycles. When the swallow(s) counter finishes counting the MOD switches to logic "1" and the prescaler changes to the divide by n mode (divide by 32 or divide by 47) for the remaining p-s clock cycles. During this mode, since swallow(s) counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0", thus saving the switching power in swallow(s) counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band 0 to 48 for the higher band of operation.

B. PROGRAMMABLE COUNTER

The programmable counter is a 7-bit asynchronous down counter which consists of 7 loadable bit cells and additional logic gates. Here, bit P6 is tied to the SEL signal of the multi modulus prescaler and bits p6 and p5 are always at logic "1". The remaining bits can be externally programmed from 75 to 78 for the lower frequency band 105 to 122 for the upper frequency band. when the programmable counter finishes counting down to zero logic divide (LD) switches to logic"1"during which the output of all bit-cell in swallow counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=0) where the programmable divider get rest to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33(N/(N+1)) dual-modulus prescaler is used, a 7-bit programmable counter is needed for the low-frequency band (2.4 GHZ). Thus, the multi-modulus 32/33/47/48 prescaler eases the design complexity of the p-counter.

V. SIMULATION RESULTS

The simulations of the design are done in CAD IUS. The operation clock frequency used for simulation is 6GHZ.

A. simulation result of 2/3 prescaler

If MC=1,the output is divided by 2 else the output is divided by 3.

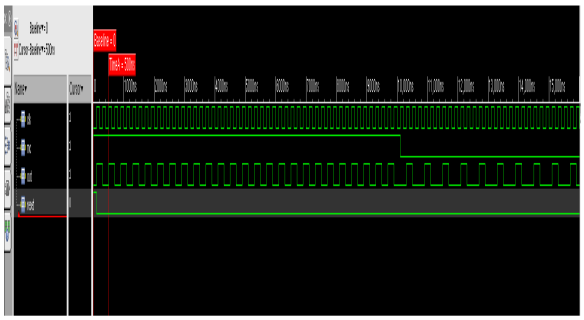

Figure5 PRESCALER 2/3

B. simulation results of multi-modulus

The multi-modulus is 32/33/47/48/64. If MOD=1,SEL=1 the output is 32, if MOD=0,SEL=1 the output is 33,if MOD=0,SEL=0 the output is 47,if MOD=1,SEL=0 the output is 48,if MOD=1,SEL=1 the output is 64.

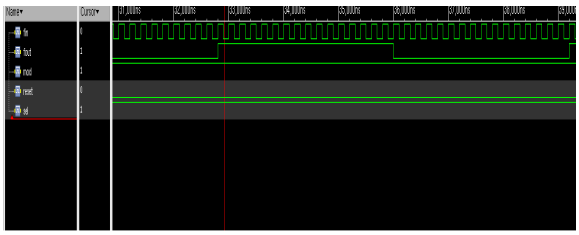

Figure6 divide by 32

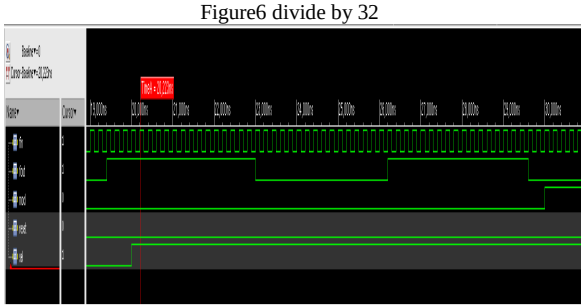

Figure7 divide by 33

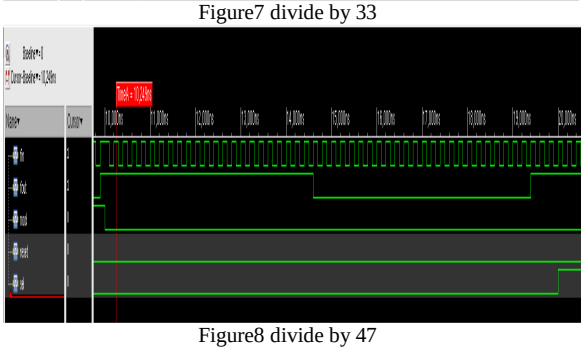

Figure8 divide by 47

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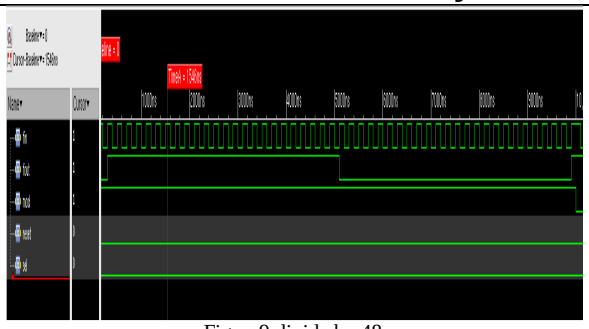

Figure9 divide by 48

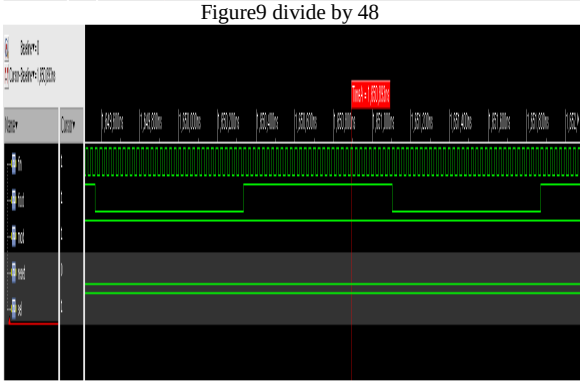

Figure10 divide by 64

VI. RESULT OF SOC AND RTL SYSNTHESIS

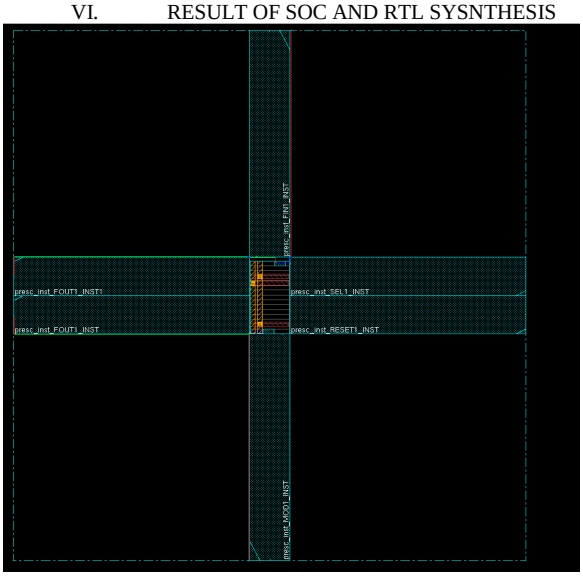

Figure11. Chip design of multi-modulus in soc

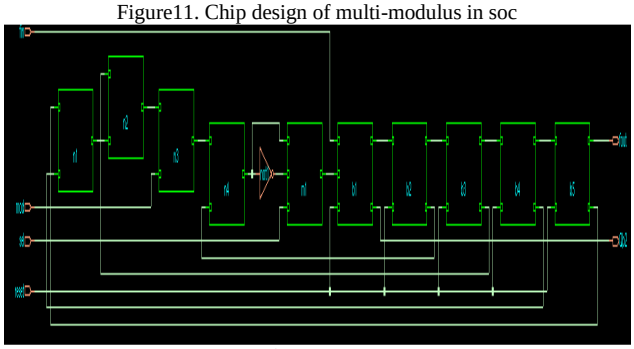

Figure12. Block diagram of multi-modulus in cadence encounter

Above shows the block diagram of multi-modulus after RTL synthesis in cadence encounter register transfer level (RTL) abstraction is used in hardware description languages (HDLS) like verilog to create high level representations o circuit from which level representations and ultimately actual wiring can be derived.

Here creating LEF file for multi-modulus attracting the LEF file for multi-modulus which gives reduced power and without attaching the LEF file multi-modulus shows the result. Top modulus of multi-modulus with and IOPAD programming in RTL encounter.

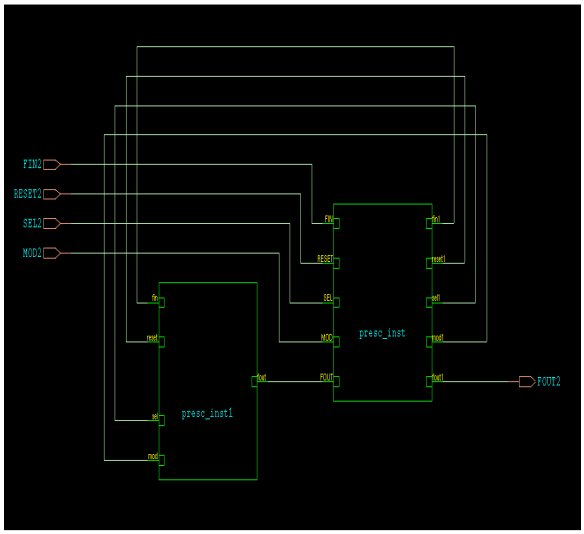

Figure13. Multi-modulus in RTL encounter

The block diagram of multi-modulus top module in which multi-modulus with RTL synthesis and multi-modulus with iopad programming is done in order to secure multi-modulus from damage in the chip.

Simulated power analysis

Simulation	*Leakage power(nw)*	*Dynamic power(nw)*	*Total power*
Multimodulus	*0.000*	*20.250*	*20.250*

IV. CONCLUSION

In this paper a simple approach for the low power single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of reload able bit cells for P and S Counter is given P and S counters can be programmed accordingly for the required bands of frequencies. Here the clock divider uses a wide band 2/3 prescaler and a multi module's prescaler. By using this multi module's prescaler, the Clock Jitter can be avoided.

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