International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

A survey on Multilevel converters in Inversion

Nagaraju. Gaddam
Assistant Professor, Dept of ENTC
SVERI's College of Engineering
Pandharpur, Sholapur, Maharastra

Dara Sampathkumar
Assoc Professor, Dept. of ECE
Vaageswari College of Engineering
Karimnagar,Telangana

Abstract- **Multilevel inverters have become more popular over the years in electric high power applications by providing fewer disturbances and functioning at low switching frequencies when compared with conventional two level inverters. In this paper presents various multilevel inverter topologies are presented such as NPCMLI, CCMLI, CMCI, MMI. All of these compared with conventional two level inverters in simulation and investigated advantages of using multilevel inverters.**

Key Terms- **Multilevel inverters, Modulation, voltage balance, comparison, PWM, topologies.**

INTRODUCTION

Conventional two-level inverters, seen in Figure 1.1a, 1.1b, are mostly used today to generate an AC voltage from a DC voltage.

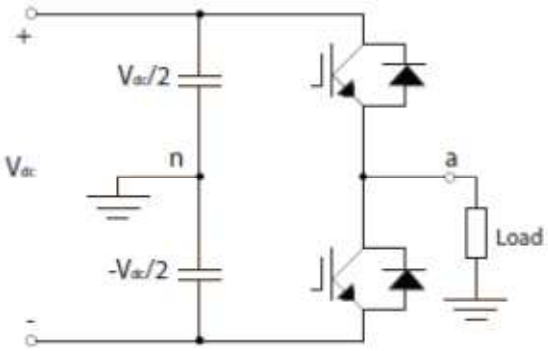


Fig 1.1a: One phase leg of a two-level inverter

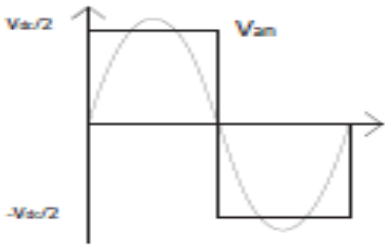


Fig 1.1b: A two-level waveform without PWM

The two-level inverter can only create two different output voltages for the load, $\frac{Vdc}{2}$ or $-\frac{Vdc}{2}$. To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 1.2.

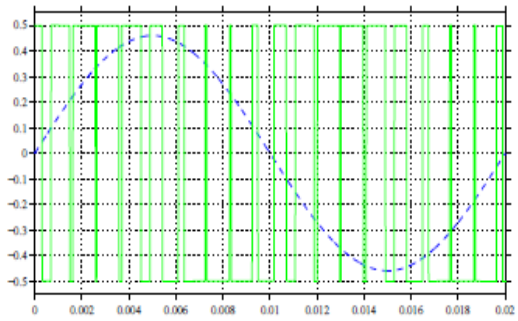


Fig 1.2: PWM voltage output, reference wave in dashed blue

Though this method is effective it creates harmonic distortions in the output voltage, EMI and high $\frac{dv}{dt}$ [2]. This may not always be a problem but for some applications there may be a need for low distortion in the output voltage. The concept of Multilevel Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 1.3, with lower $\frac{dv}{dt}$ and lower harmonic distortions.

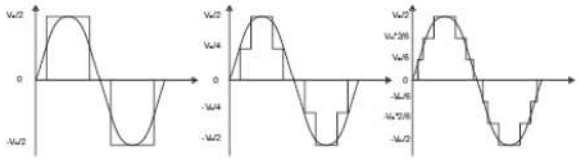


Fig 1.3: A 3-level, 5-level, 7-level waveform

With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

To better understand multilevel inverters the more conventional three-level inverter, shown in Figure 1.4, can be investigated.

It is called a three-level inverter since every phase-leg can create the three voltages $\frac{Vdc}{2}$, 0, $-\frac{Vdc}{2}$, as can be seen in the first part of Figure 1.3. A three-level inverter design is similar to that of a conventional two-level inverter but there are twice as many valves in each phase-leg. In between the upper and lower two valves there are diodes, called clamping diodes [1], connected to the neutral.

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

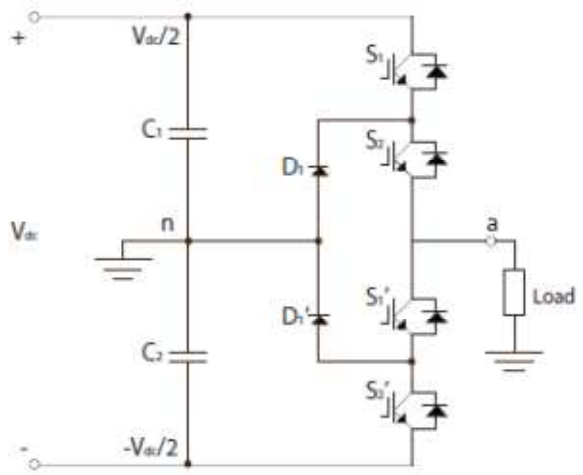


Fig 1.4: One phase leg of a 3-level inverter

Midpoint in between two capacitors, marked n in the figure. This capacitor build up the DC-bus, each capacitor is charged with the voltage $\frac{Vdc}{2}$. Together with another phase-leg an output line-to-line voltage with even more levels can be obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure 1.3, the result is a multilevel inverter with clamping diode topology. Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and $\frac{dv}{dt}$, generate smaller common-mode voltage and operate with lower switching frequency [2] compared to the more conventional two-level inverters. With a lower switching frequency the switching losses can be reduced and the lower $\frac{dv}{dt}$ comes from that the voltage steps are smaller, as can be seen in Figure 1.3 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, topologies with different properties have been developed, some of which will be looked upon in this paper. The Multilevel inverter topologies that are investigated in this work are: Neutral- Point Clamped Multilevel Inverter (NPCMLI), Capacitor Clamped Multilevel Inverter (CCMLI), Cascaded Multi cell Inverter (CMCI), Modular Multilevel Inverter (MMI).

MULTILEVEL DIODE CLAMPED/NEUTRAL POINT INVERTER (NPCMLI)

According to patents the first multilevel inverter (MLI) was designed in 1975 and it was a cascade inverter (cascaded inverters will be presented in a later chapter) with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter, also called Neutral-Point Clamped Inverter (NPC) [2], see Figure 2.1.

This topology is, as can be seen from the figure, based on the same principal as the before mentioned three-level inverter in Figure 1.4. In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line, see the left part of Figure 2.1. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an (m-1) number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate).

In Figure 2.1 one phase-leg of a five-level NPC inverter is displayed. By adding two identical circuits the three phase-legs can together generate a three-phase signal where Sharing of the DC-bus is possible. The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. For example, in Figure 2.1 all diodes are rated for $\frac{Vdc}{4}$ ($\frac{Vdc}{m-1}$in general) and the D_1' diodes need to block $3\frac{Vdc}{4}$ and therefore there are three diodes in series. However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. With this configuration five levels of voltage can be generated between point a and the neutral point n; $\frac{Vdc}{2}$, $\frac{Vdc}{4}$, $0, -\frac{Vdc}{4}$ and $-\frac{Vdc}{2}$, depending on which switches that are switched on.

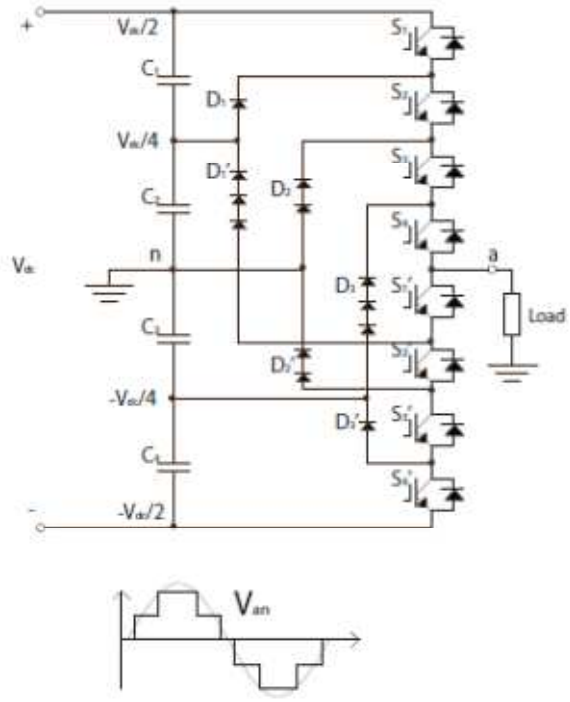


Fig 2.1: One phase leg for 5-level NPC inverter

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

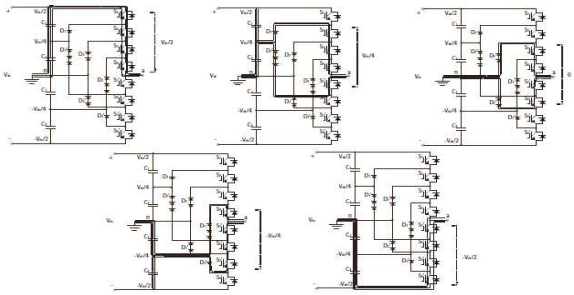
A waveform from one phase-leg of the inverter can also be seen in Figure 2.1 in which the steps are clearly visible. For NPCMLIs with a higher number of voltage levels the steppes will be smaller and the waveform more similar to a sinusoidal signal.

Output Voltage	S1	S2	S3	S4	S'1	S'2	S'3	S'4
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

Table 2.1: switching states of one five level phase leg, 1 means turned ON, 0 means turned OFF

In Table 2.1 the different states for the five-level NPC inverter are shown. Note that there is the possibility to only turn on (and off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a fundamental switching frequency. From Table 2.1 it can be seen that for the voltage $\frac{Vdc}{2}$ all the upper switches are turned on, connecting point a to the $\frac{Vdc}{2}$ potential, see Figure 2.2.

For the output voltage $\frac{Vdc}{4}$ switches S_2, S_3, S_4 and S'_1 are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and D'_1. For voltage levels $-\frac{Vdc}{4}$ or $-\frac{Vdc}{2}$ clamping diodes D_2 and D'_2 or D_3 and D'_3 hold the voltage, respectively. For the voltages $\pm\frac{Vdc}{2}$ the



current, when both voltage and current are positive (positive current goes out from the inverter), goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the D_x diodes and negative current through the D'_x diodes and also through the switches in between the clamping diodes and the load. For example, for state $\frac{Vdc}{4}$ positive current goes through diode D_1 and switches S_2, S_3 and S_4. In Figure 2.2 the turned on switches for every state are shown, switches in parallel to the thick dashed lines are on. In the figure the current paths are also shown, thin dashed lines, for every state and for both positive and negative current. For example for the $\frac{Vdc}{2}$ state the switches (positive current) or the diodes (negative current) are conducting and for the $\frac{Vdc}{4}$ state the current goes either through D_1 and three switches (positive current) or D'_1 or through one switch (negative current). If there is a DC-source charging the DC-bus there is an also current flowing through the DC-bus to keep the DC-bus voltage constant. Table 2.1 also shows that some switches are on more frequently than others, mainly S_4 and S'_1, as long as a sinusoidal output wave that requires the use of all voltage levels is created. When the inverter is transferring active power this leads to unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads and that current is drawn from nodes between capacitors. The total DC-bus voltage will be the same but the capacitors voltage will deviate from each other. While transferring real power current is drawn from, for example, capacitor C_1 and C_2 during different amount of time, as can be seen in the left part of Figure 2.3. The time intervals in the figure represent the discharge time and as can be seen C_2 is discharged more, leading to unequal capacitor voltages. Also, during for example the $\frac{Vdc}{2}$ state current discharges both C_1 and C_2 but in the $\frac{Vdc}{4}$ state current is drawn from the point between C1 and C_2, discharging C_2 but charging C_1. This makes the voltages over the capacitors to deviate in a special way. When only transferring reactive power however the NPCMLI does not have this voltage unbalancing problem [3], see right part of Figure 2.3.
This is because of that time intervals during which the capacitors charged and discharged are equal during reactive power transfer, as the figure suggests.

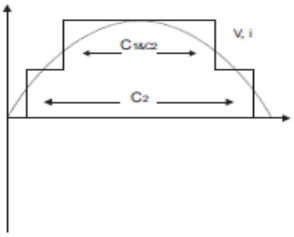


Fig 2.3a: When voltage and current in phase

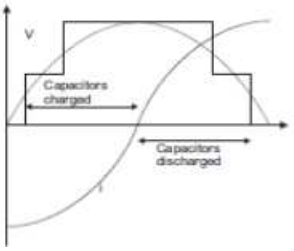


Fig 2.3b: when voltage and current 90º out of phase

MULTILEVEL CAPACITOR CLAMPED/FLYING CAPACITOR INVERTER (CCMLI)

A similar topology to the NPCMLI topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, which can be seen in Figure 2.4.
Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. As for the NPCMLI, m-1 number of capacitors on a shared DC-bus, where m is the level

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

number of the inverter, and 2(m-1) switch-diode valve pairs are used. However, for the CCMLI, instead of clamping diodes, one or more, capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position on each side of the midpoint between the valves [3], see capacitors C_1, C_2 and C_3 in Figure 2.4.

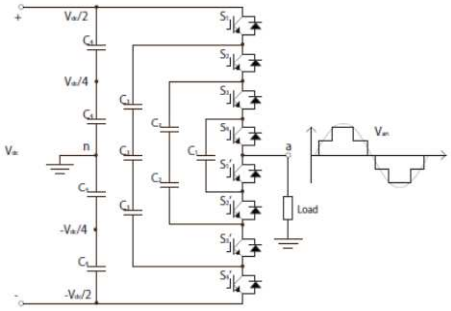


Fig 2.4: A five level Capacitor clamped MI

As can be noticed in Figure 2.4 the same number of main switches, main diodes and DC-bus capacitors as in the NPCMLI are used for the CCMLI. The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages the number of switching combinations increases [3]. Several switching states will be able to generate the same voltage level, giving the topology redundant switching states. The sum of a certain output voltage is generated by the DC bus voltage $\pm \frac{Vdc}{2}$ and one or more of the clamping capacitors voltages added together. Since every capacitor is rated for the voltage $\frac{Vdc}{4}$ (in this five-level case, V_{dc} m-1 in general), DC-capacitor and clamping capacitor alike, the output voltage, for this example $\frac{Vdc}{4}$, is generated by the DC-bus positive top value ($\frac{Vdc}{2}$) and the reverse voltage of clamping capacitor C1. The other voltage states work in similar ways but with the help of other clamping capacitors.

Output Voltage	S1	S2	S3	S4	S'1	S'2	S'3	S'4
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
-Vdc/4	1	0	0	0	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

Table 2.2: Switching states for five level CCMI

Table 2.2 shows some switching states for a five-level CCMLI and Figure 2.5 shows an alternative to the state giving zero voltage in the table. In the figure the dashed line represent the path the current flows from the neutral point to the load. It flows through two C_4 capacitors, giving $\frac{Vdc}{2}$ potential, then through switch S_1 and down the C_3 capacitors. Since every capacitor is charged with the voltage $\frac{Vdc}{4}$ the potential is now lowered with $3\frac{Vdc}{4}$ the current the flows up through the diodes in parallel with the switches $S_3'$and S_2' and through capacitor C_1 and then out to the load through switch S_4 with the resulting potential 0 Volt. As before with the NPCMLI only one switch need to be opened and one to be closed to change one state to another. This leads to that the inverter can be modulated at low (fundamental) switching frequency since a stepped sinusoidal waveform can be created when every switch is turned on and off only once per output frequency cycle. Also, as mentioned, the states shown in Table 2.2 are not the only states that put out these voltages; there are several switching states for all of the voltage levels, except the $\pm\frac{Vdc}{2}$ states. Depending on what state is chosen the capacitors can charge or discharge each other, making it possible to balance the charge in the capacitors with control methods [2]. Since the same current flows through all the active capacitors in a state, energy can be transferred from more charged to less charged capacitors, balancing the capacitors

Voltages between the capacitors that are conducting. If a method of using redundant switching states for voltage balancing is not applied there will be a capacitor voltage balance problem when transferring active power. However, if such a method is used the switching frequency may need to be raised for the balancing to be achieved properly [3].

The reason the capacitors voltages to get unbalanced while transferring active power some states are on during a longer time and the active capacitors gets discharged or charged more than others, much like in Figure 2.3. The unequal workload cause voltage unbalance but by using the redundant switching states the unbalances can be controlled. For pure reactive power transfer the CCMLI does not have any voltage balancing problem, which is also explained with Figure 2.3. Capacitors are charged and discharged equally during one cycle while transferring reactive power, like with the NPCMLI.

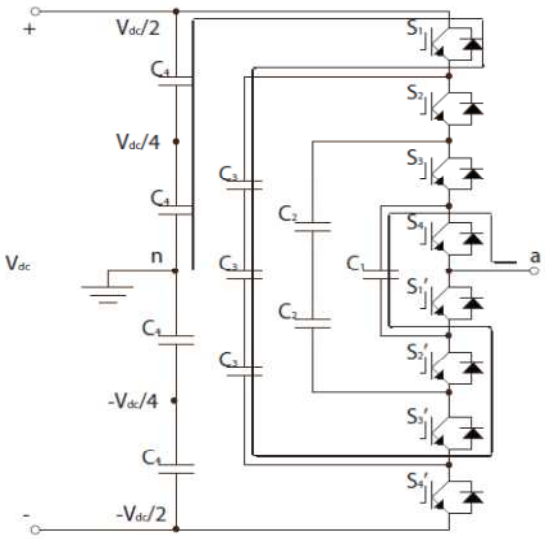


Fig 2.5: One example of a alternative switching state for the voltage 0.

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

The amount of components for the CCMLI topology is as stated very similar to the NPCMLI, m-1 number of capacitors on a shared DC-bus and 2(m-1) switch-diode valve pairs, but with the deference that CC topology uses clamping capacitors instead of diodes. These capacitors do, as the diodes did, grow in numbers quadratic ally with the voltage level m, following the equation $\frac{(m-1)\times(m-2)}{2}$ [2], not counting the main capacitors on the DC-bus. Again the need for several components of the same sort and rating in series is needed because of the high voltage ratings, as for the clamping diodes in the NPCMLI. When the CCMLI is used in a three-phase setup it can, as the NPCMLI, share the DC-bus and only multiply all the other remaining components by three.

CASCADED MULTI CELL INVERTER (CMCI)

A Cascaded Multi cell Inverter (CMCI) differs in several ways from NPCMLI and CCMLI in how to achieve the multilevel voltage waveform. It uses cascaded full-bridge inverters with separate DC-sources, in a modular setup, to create the stepped waveform.

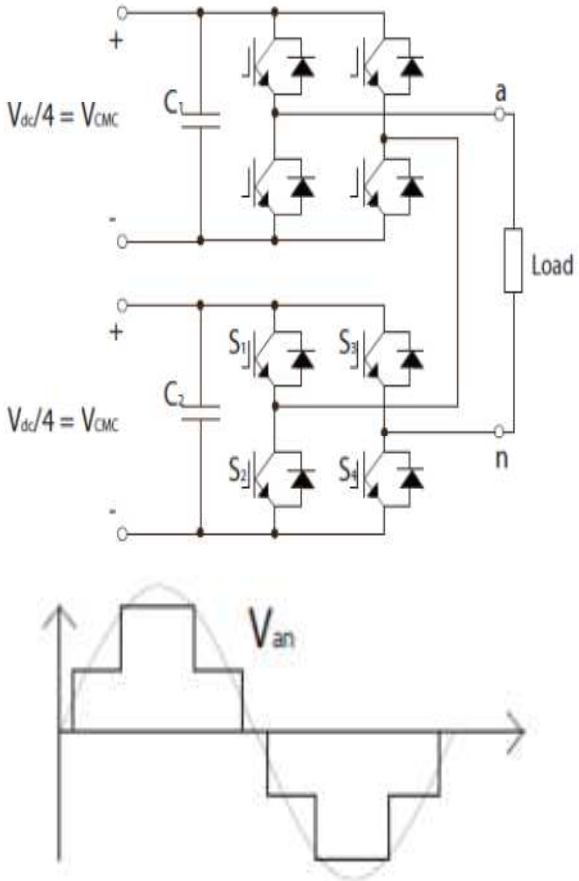


Fig 2.6: A five-level cascaded multi cell inverter

In Figure 2.6 one phase-leg of a five-level Cascaded Multi cell Inverter is shown. Each full-bridge can be seen as a module and it is only these modules that build up the CMCI topology. One full-bridge module is in itself a three-level CMCI, and every module added in cascade to that extends the inverter with two voltage levels. In Figure 2.6 there are two full-bridge modules creating the five different voltage levels available. Applications suitable for the CMCI are for example where photovoltaic cells, battery cells or fuel cells are used [3]. Such an example could be an Electric Vehicle there several power cells exists. The total output voltage is the sum of the outputs of all the full-bridge modules in the inverter and every full-bridge can create the three voltages V_{CMC}, 0 and $-V_{CMC}$. To change one level of voltage in the phase output the CMCI turns one switch on (and one o_) in one full-bridge module. For a full-bridge module to add the voltage V_{CMC} the switches $S_1$and S_4 are turned on, for $-V_{CMC}$ the switches S_2 and S_3 are turned on. When there is current flowing through the full-bridge the 0 voltage is achieved by turning on the two switches on the upper halves of the full-bridge (S_1 and S_3) or the two switches on the lower part (S_2 and S_4). Together with several full-bridges a stepped waveform can be generated. The maximum output voltage is $\frac{m-1}{2}V_{CMC}$ = s V_{CMC} = $\frac{Vdc}{2}$ (and minimum voltage $\frac{m-1}{2}(-V_{CMC})$ = s$(-V_{CMC})$ = $-\frac{Vdc}{2}$), where m is the number of levels and s the number of full-bridge modules[2]. It should be noted that the CMCI is capable of putting out the total voltage source magnitude in both positive and negative direction while many other topologies can only put out half the total DC-bus voltage source magnitude. This is why the total sum of the DC-side voltages in Figure 2.6 is Vdc 2 and not Vdc, since it is still able to put out Vdc 2 to the output (like the other topologies). All full-bridge inverters that are connected can contribute with the same voltage, in a way making the topology very scalable. There is also the possibility to charge every module with different voltages. The sources in each full-bridge need to be isolated if the inverter is going to be implemented in a active power transfer application, for voltage balance reasons since there is no common DC-bus to recharge the sources energy content. However, since the CMCI uses separate energy sources it is well suitable for renewable energy or energy/fuel cell
Applications there every separate voltage source could be isolated [3]. A drawback for the energy/fuel cell applications is however that the sources must be charged individually or through the inverter. Still, the charge balance in the voltage sources needs to be controlled, for example in electric vehicle batteries, so that there is no voltage unbalance, but this can be done with balancing modulation methods. Balancing modulation methods will be investigated further in chapter 4. When adapted to pure reactive power applications the CMCI is self balanced, just as the NPCMLI and CCMLI, since the charge change over one cycle is zero [3] (right part of Figure 2.3). Since there is no common DC-bus to recharge the sources in the CMCI topology, balancing modulation strategies
include prioritizing higher charged modules in modulation (see chapter 4) or activating two modules not needed for the output voltage level and let them balance each other

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

(transferring energy from higher charged module to lower charged module). Two modules for balancing purposes are only available when the output voltage level is two levels lower than maximum (zero voltage level for the five-level MLI) or more. When two modules are available in this way one of the can be activated with positive voltage and the other with negative voltage. The resulting output voltage of these two modules is then zero but energy is transferred from the positive module to the negative module when current goes out from the inverter (and the other way around when current goes into the inverter).

In this way two modules can balance each other when they are not needed for generating the output voltage. Compared to the NPCMLI and CCMLI the CMCI requires fewer components, every voltage level requires the same amount of components. However, the number of sources is higher, for the phase-leg to be able to create a number of m voltage level s = $\frac{m-1}{2}$ sources are required [4]. The number of sources s is also equal to the number of full bridge modules. In turn, every full-bridge module has four diodes and four switches in turn giving the CMCI $4\frac{m-1}{2}$ = 2(m-1) = 4s diodes and switches. When making a three-phase inverter with the CMCI topology the number if needed components needs to be multiplied by three for all components since there is no common DC-bus to share.

MODULAR MULTILEVEL INVERTER (MMI)

The Modular Multilevel Inverter (MMI), seen in Figure 2.11, is a newer topology first introduced in 2002 [8].It uses a modularized setup of sub modules, essentially half bridges, which are connected or bypassed to generate a certain output voltage level. Every phase-leg is composed of two arms where each arm has a number of n sub modules. In turn, in every sub module there is a DC-capacitor charged with the voltage V_{MMI} = $\frac{Vdc}{m-1}$ each arm can then generate the maximum voltage of ±n×V_{MMI} =±Vdc, where the modules in both arms are connected or bypassed to create a AC output voltage. So for a number of voltage levels m the inverter needs m-1 = n number of sub modules per arm, so 2(m-1) = 2n sub modules per phase-leg. Compared to the somewhat similar C_{MCI} topology the modules in this MMI topology can only put out two voltages, V_{MMI} or 0.

This explains the need for two arms in every phase-leg. The MMI topology does not need shared DC-capacitors in a DC-bus, but does however require a DC-bus for circulating currents. These currents can however also circulate through other phase-legs. The two inductors, one in each arm in a phase-leg, are there to take up the voltage difference when modules are switched in and out. To activate a certain sub module in a phase-leg arm to make its voltage source contribute to the output voltage the switch S_1 is switched on and S_2 is switched off.

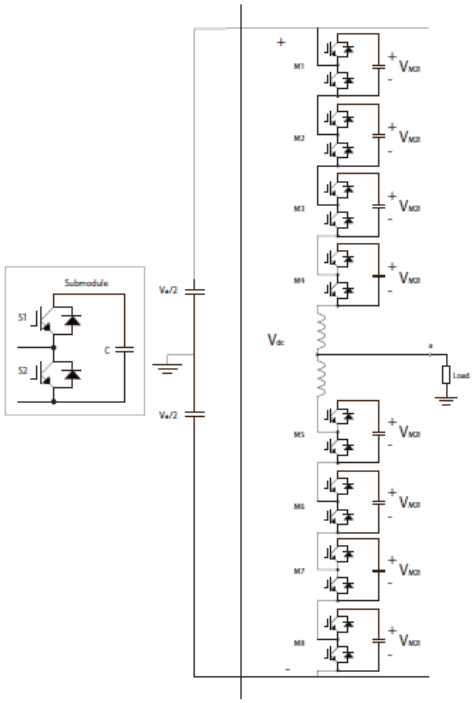


Fig 2.11: One phase leg of a five level MMI

To bypass a sub module the switches S1 is turned off and S2 is turned on in that certain sub module. The arm in which a sub module is to be connected is determined by if they wanted voltage is positive or negative and which sub module in the arm is determined by the balancing modulation. The balancing modulation is the program that chooses which modules that are to be activated for each state to achieve voltage balance in all modules. To keep the sources in the sub modules balanced the order in which they are connected can be changed. If, for instance, one sub module has more charge stored in its capacitor it can be prioritized to be activated first or last, depending on current direction, to balance the sub module voltages. The MMI topology hence has a redundant setup of switching states. Some switching state examples for achieving the voltage levels in this five-level MMI can be seen in Table 2.4.

Vload	M1	M2	M3	M4	M5	M6	M7	M8
Vdc/2	0	0	0	0	1	1	1	1
Vdc/4	1	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1
-Vdc/4	1	1	1	0	0	0	0	1
-Vdc/2	1	1	1	1	0	0	0	0

Table 2.4: Switching states of a MMI

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

Note that during any moment, half the modules are connected and half the modules are bypassed. This is necessary since the sum of all connected modules in a phase-leg must be Vdc. Component requirements for the MMI topology is mostly dependent on the number of sub modules, and hence the number of voltage levels, since there is only the inductor in the topology setup that is independent of the number of levels. Every sub module is composes of a half-bridge and a DC-capacitor, so for every sub module there is two switches, two diodes and one capacitor. Additionally, for every phase-leg there are two inductors for the phase-leg arms. The inductors, seen close to the midpoint in the phase leg in Figure 2.11, are there to take up the voltage difference between states. Also, each switch in the MMI sub modules must be able to withstand at least the sub module capacitor voltage, VMMI. Since the voltage spanning over both arms is Vdc and the number of sub modules in the arms, as a function of number of voltage levels, is m-1 the voltage that a switch must be ble to withstand described with the total DC voltage is$\frac{Vdc}{m-1}$.

Modulation When it comes to multilevel inverter modulation there are basically two groups of methods:
Modulation with fundamental switching frequency or high switching frequency PWM [2]. For both cases a stepped output waveform is achieved, but with the high switching frequency methods the steppes are modulated with some sort of PWM. Independent of switching frequency choice there are, however, also space vector methods to choose from. 3.1 PWM for two-level inverters Ordinary PWM modulation for two-level inverters is accomplished through comparison between a reference wave and a triangular carrier wave.

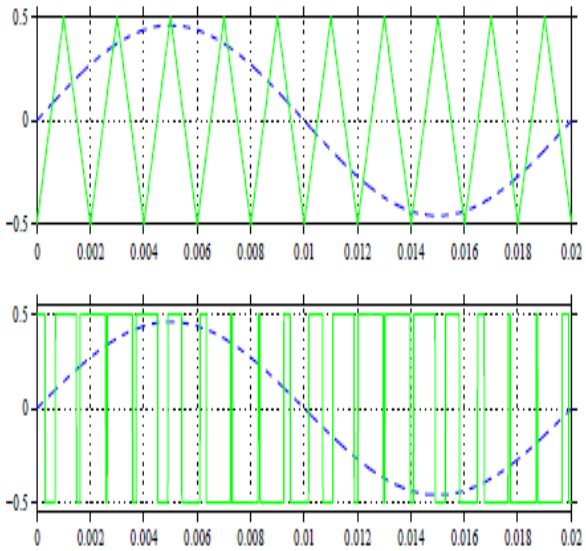


Fig 3.1: PWM reference and triangular carrier

The reference wave have the frequency and amplitude wanted for the output voltage signal and the triangular carrier wave has the amplitude of half the DC input voltage, in an simple ordinary case, and its frequency is dependent on application but must be higher than the reference wave frequency. In electric power application the carrier wave frequency is often in the range of kHz. The reference wave frequency decides how often the switches in the inverter changes state, every time the triangular carrier wave crosses the reference wave the switches turn on or off. A plot of the ordinary two-level PWM reference, carrier wave and output voltage can be seen in Figure 3.1. If the carrier wave crosses the reference so it becomes higher than the reference the top switch turns off and bottom switch turns on in the two level inverter (see Figure 1.1) so that $\frac{Vdc}{2}$ becomes the output. When the carrier wave crosses the reference again, now getting lower than the reference, the switches change state and the output becomes $-\frac{Vdc}{2}$. When the reference is positive the output voltage signal will be $\frac{Vdc}{2}$ for the majority of the time resulting in a positive output AC signal following the reference. An straightforward example is if the reference wave is constant at zero voltage, the carrier wave would then cross it upwards and downwards with the same time between every crossing, making $\frac{Vdc}{2}$ and $-\frac{Vdc}{2}$ being the output for equal time, each cycle. This leads to that the average output voltage over one carrier wave period becomes zero.

PWM FOR MULTILEVEL INVERTERS

Multilevel PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave, much like in the two-level PWM case. To reduce harmonic distortions in the output signal phase-shifting techniques are used [2]. There are several methods that change disposition of or shift multiple triangular carrier waves. The number of carrier waves used is dependent to the number of switches to be controlled in the inverter.

PHASE SHIFTED CARRIER PWM

The Phase Shifted Carrier PWM (PSCPWM), Figure 3.2, is a multicarrier modulation strategy that has all carrier waves phase shifted from each other. It is the standard modulation strategy for the CMCI topology [10] but is not exclusively for that topology. For a CMCI with n number of full-bridge modules in each phase-leg there are also n number of triangular carrier waves. There is one triangular carrier wave for each full bridge module, phase shifted with 180_
n in between them, with amplitudes the magnitude of the total DC voltage. The magnitudes for the carrier waves are modulated by the actual voltage level in the appropriate module. For the five-level CMCI with two modules there are two triangular carrier waves, one for each module, see Figure 3.2.
The modules create the two voltages in Figure 3.3 with PSCPWM modulation. There are also two reference waveforms for the two legs in each inverter modules that are phase shifted 180° from each other, as can be seen in Figure 3.2.

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

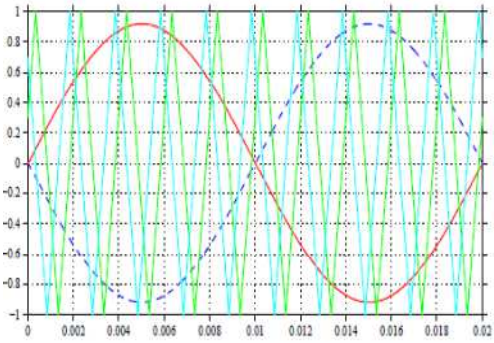


Fig. 3.2: Carrier and reference waves for Five-level CMCI

Both reference waves are compared with both carrier waves, one reference wave is for modulation of the left full-bridge module leg switches (dashed reference wave) and the other reference wave to modulate the right full-bridge
Module leg switches (solid reference wave).

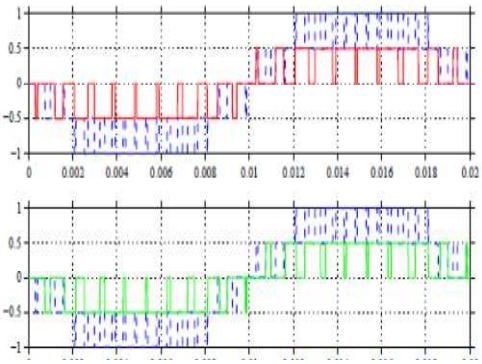


Fig 3.3: Two model voltages

The first triangular wave in Figure 3.2 is compared with the upper output voltage plot in Figure 3.3 (and the second triangular with the lower voltage plot). Close to 2ms in the plots it can be seen that the first triangular wave crosses one reference wave downwards, controlling the right leg switches of the modules, and turning that modules output voltage from 0 kV to -0.5 kV. Closely after the second carrier wave crosses the same reference wave (the one that controls the right leg switches in the modules) upwards turning the output voltage from -0.5 kV to 0 kV. Comparisons with the other reference wave works in the same wave, but then controlling switches in the modules left legs. As the plot suggests the two modules share the workload for all levels, no module is strictly connected to one voltage level in the output. For the CMCI this strategy cancels all carrier and sideband associated harmonics up to the 2nth carrier group [6].

PHASE DISTORTION PWM

In Phase Distortion PWM (PDPWM), Figure 3.4, all carrier waves are in phase. A great acknowledgment for this technique is that it is generally accepted as the method that creates the lowest harmonic distortion in line-to-line voltage [7].

When used for an NPCMLI with m number of voltage levels, m-1 numbers of triangular carrier waves are used.

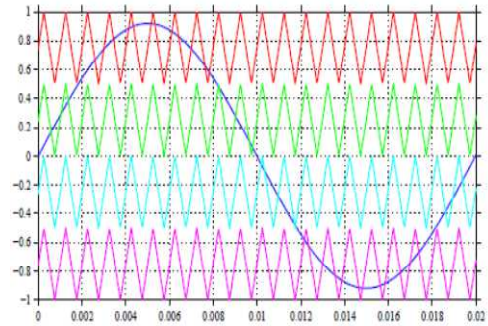


Fig 3.4: The reference (cosine) and carrier waves (triangular) for a five-level NPCMLI Or CMCI with PDPWM

These carrier waves have the same frequency and are arranged on top of each other, with no phase shift, so that they together span from maximum output voltage to minimum output voltage [6]. The carrier waves amplitudes should be modulated with aspect of the current voltage magnitude for each respective voltage level; each carrier wave is connected to a specific output voltage level. If the carrier waves are not modulated in this way the correct output voltage will not be achieved if the sources voltage levels change from their supposed value (get unbalanced). If the sources voltage amplitudes change without that the carrier waves are modulated with that change the
Correct output voltage will not be generated during the during the correct time spans. When one carrier wave is crossed by the reference the output wave steps one level up or down with a switch transaction. One carrier wave hence modulates the use of one voltage state. Only one level is modulated at any time, as can be seen in the in Figure 3.4, since the reference only crosses one carrier at any level. The output voltage from the PDPWM modulation with a five-level NPCMLI is shown in Figure 3.5. The carrier waves should be modulated with aspect of the current voltage magnitude for each respective voltage level.

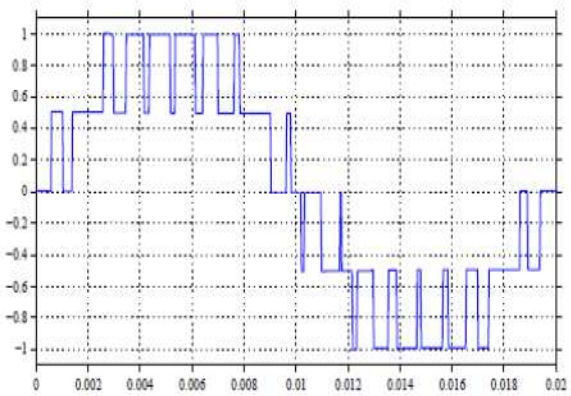


Fig 3.5: The output voltage for a five-level NPCMLI with PDPWM

Phase Distortion PWM is also the proposed control method for the RVMLI [5] but can be used with other topologies as well. For the CMCI the PDPWM modulation is built up of m-1

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

carrier waves, two for each full-bridge module, one below zero and one above zero for every module. Each module then modulates one voltage level. Which level one full-bridge module modulates can be changed for balancing purposes. For the five-level CMCI this could mean that the module with highest charge within its source is modulated by the carrier waves two and three in Figure 3.4, if counting the carrier waves from top to bottom. The other module, with lower charge, would then be controlled by Carrier waves one and four. Since waves two and three are closest to zero the first module, with higher charge, will be connected to the load first every half cycle, for both positive and negative output voltages. This will lead to a higher workload for this module. If which module contains the most charge change, the modules can change which carrier waves that modulate them with each other. More generally, the two triangular wave's closes to zero (one wave with positive voltage and one with negative voltage) can control the module with the highest charge if active power is to be transferred. The positive carrier then modulated the full-bridge modules left leg for positive output voltages and the negative carrier the right leg for negative output voltages. Other modules should be controlled by two carrier waves further away from zero, one from each side of zero voltage at the same position (second wave above and second wave below zero, for example). The carrier waves amplitudes should be modulated by the voltage level in the full-bridge module it controls, much like with the carrier wave modulation for PSCPWM, so that correct output voltages are generated during the correct time spans.

SELECTIVE HARMONIC ELIMINATION (SHE)

Selective Harmonic Elimination is a low switching frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage? With the help of Fourier series analysis the amplitude of any odd harmonic in the output signal can be calculated. Usually the switching angles are chosen so that the fundamental is set to the wanted output amplitude and the other harmonics to zero see Figure 3.7. The switching angles must however be lower than $\frac{\pi}{2}$ degrees and for a number of switching angles a harmonic components can be affected, where a-1 number of harmonics can be eliminated[2] (one angle to set the fundamental). If angles were to be larger than $\frac{\pi}{2}$ a correct output signal would not be achievable. For an inverter with m levels a $=\frac{m-1}{2}$: Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. For a five-level inverter a = 2, so there are two switching angles available and a-1 = 1 angles can be used for harmonic component elimination. In Figure 3.7 the first angle, α1, is set to modulate the fundamental signal amplitude the second angle, α2, is set to eliminate a chosen harmonic distortion. The Fourier series equations for these signals are the following.

$$\frac{m_i \times V_{max} \times \pi}{4} = \frac{V_{max}}{2}\cos\alpha_1 + \frac{V_{max}}{2}\cos\alpha_2$$

$$0 = \cos(n \times \alpha_1) + \cos(n \times \alpha_2)$$

$$m_i = \frac{V_{ref}}{\sqrt{2}\ V_{max}}$$

The variable n is in these equations is the number (multiple of the fundamental frequency)
Of the harmonic that is to be eliminated. For every switch angle available one cosine term i added to each equations and there are also as many equations as there are switching angles. So for a situation with a number of switching angles there are a number of equations with a number of cosine terms. As for this five-level inverter case there are two firing angles, two equations and two cosine terms in every equation. For a seven-level inverter the equation setup would instead be as the following. Variables n_1 and n_2 are the numbers of the two harmonics to be eliminated.

$$\frac{m_i \times V_{max} \times \pi}{4} = \frac{V_{max}}{3}\cos\alpha_1 + \frac{V_{max}}{3}\cos\alpha_2 + \frac{V_{max}}{3}\cos\alpha_3$$

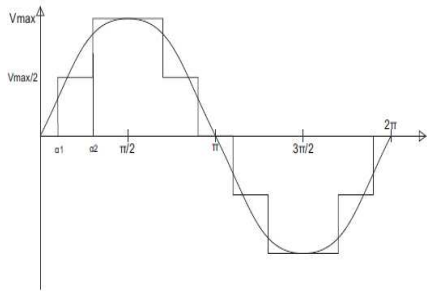


Fig 3.7: Switching with angles

$$0 = \cos(n_1 \times \alpha_1) + \cos(n_1 \times \alpha_2) + \cos(n_1 \times \alpha_3)$$
$$0 = \cos(n_2 \times \alpha_1) + \cos(n_2 \times \alpha_2) + \cos(n_2 \times \alpha_3)$$

POWER LOSSES

Losses are an important aspect of power electronics since lower losses gives higher efficiency. Since the two-level and multilevel inverters can operate at different switching frequencies and with different balancing control schemes they will not have the same amount of
power losses. To be able to investigate the switching losses in an inverter a model for losses is needed. The switching power loss Psw during one second in a switch is defined by the formula

$$P_{sw} = \sum \frac{1}{2} V_d I_0 t$$

there Vd is the voltage over the switch when off, I0 is the current through the switch after turned on or before turned off and t is either the turn on time ton or the switch off time toff

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

[9]. The sum of all the switching loss event energies during one second for one switch results in that switch's switching power loss. The switching loss energies can be divided into the turn on and turn off loss energies as

$$E_{sw,on} = \frac{1}{2} V_d I_0 t_{on}$$

$$E_{sw,off} = \frac{1}{2} V_d I_0 t_{off}$$

During one second $E_{sw;on}$ and $E_{sw;off}$ are lost a number of f_{sw} times, where f_{sw} is the switching frequency of the switch, so the sum of the switching energy losses equals the switching power losses. Also the number of switches in a circuit has to be included.

$$P_{sw} = \sum (E_{sw,on} + E_{sw,off}) = \sum E_{sw,tot}$$

$$P_{sw,tot} = N_{sw} \sum (E_{sw,on} + E_{sw,off} = N_{sw} \sum E_{sw,tot}$$

Where Nsw is the number of switches in the inverter. For these equations it is assumed that the same voltage lies over all switches and also that the same current flows through them. Both voltage and current used for with these equations are values measured every sampling instance during simulations. Since voltages and currents does not change between sampling instances during simulations the current I0and voltage Vd can be assumed to be constant for every term in the sum calculations. Diodes, like clamping diodes or those in parallel with switches, also have turn off losses that needs to be included. Also, when the current is negative (positive current down through switch) the current goes through the diode in parallel to the switch and the switch has no losses. The diode turn off energy loss is similar to that of the switch. There are also conduction losses in the semiconductor devices. These are not dependent on the inverter switching frequency but on the voltage over and current through the device. The on-state resistance in the devices is also important for conduction loss calculations. For a time t_{cond} that a semiconductor is on and conduction the conduction energy losses can be calculated with

$$E_{cond} = t_{cond}(V_t I_0 + r_{on} I_0^2)$$

Where Ron is the on-state resistance and V_t the voltage over the device during on-state (threshold voltage). Also here the voltages and currents are measured at every sampling instance during a simulation and hence the currents and voltages can be assumed to be constant for each term in the sum calculation. To get the total conduction power losses for all devices during one second the conduction energies for all switches has to be summed up.

$$P_{cond,tot} = N_{sw} \sum E_{cond}$$

Strengths and weaknesses of the topologies

Because of the topologies different designs they also have separate properties that distinguish their suitability for different applications and situations. Their design and basic principle has been presented earlier in this work but for further evaluation a short and simple view on the topologies positive and negative properties could be helpful. The advantages and disadvantages are listed for every topology below.

NEUTRAL-POINT-CLAMPED MULTILEVEL INVERTER (NPCMLI)

+ High efficiency since fundamental switching frequency can be used for all devices
+ Controllable reactive power flow
+ Simple control method for back-to-back power transfer system
- High number of clamping diodes with high number of voltage levels
- Difficulties with active power flow [3]
- Capacitor Voltage Balance problem that need complex modulation

CAPACITOR CLAMPED MULTILEVEL INVERTER (CCMLI)

+ Capacitors can function as power storage during outage [3]
+ Voltage balancing with redundant switching states
+ Can control both active and reactive power transfer
- Requires many capacitors
- Complicated control, leading to high switching frequency and losses, when transferring real power

CASCADED MULTI CELL INVERTER (CMCI)

+ Requires a low number of components per level
+ Modularized structure without clamping components
+ Possibility to implement soft-switching
+ Simple voltage balancing modulation
- Needs separate isolated DC sources for real power transfer
- No common DC-bus

MODULAR MULTILEVEL INVERTER (MMI)

+ Modular design
+ Low number of components
+ Simple voltage balancing
- Many DC-capacitors

SIMULATION RESULTS AND LOSS CALCULATIONS

SIMULATION SCOPE

The two selected MLI topologies, the NPCMLI and CMCI, are compared with each other and with a conventional two-level PWM inverter to investigate the differences between multilevel technology and ordinary two-level technology. For the comparison quality issues such as harmonic components and THD are used together will calculated switching and conduction losses. The capacitor voltage balance problems have been investigated for both MLI topologies.

Simulations for the NPCMLI have concerned one pure reactive power case to examine its capability for VAR

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

compensation and one case with mixed active and reactive power transfer to investigate the topologies suitability for applications such as HVDC transmission. The CMCI topology will be tested with the same sets of simulations, pure reactive and mixed active and reactive power transfer, with concern on equal discharge of the voltage sources. For performing the simulations PSCAD v.4.2.1 is used and the simulation results are presented with the tools in Mat Lab.

SIMULATIONS MODELS AND COMPONENT VALUES

The three simulations models used are the two-level inverter, the five-level Cascaded Multi cell Inverter (CMCI) and the five-level Neutral-Point Clamped Inverter (NPC). These models can be seen in Figures 6.1, 6.2 and 6.3. The values for the two load cases, reactive power transfer and mixed power transfer, can be seen in Table 6.1.

	R (ohm)	L (H)	Va (RMS) (kV)	Ia, ideal (RMS) kA)	Pa (kW)	Qa (kVAR)
Reactive Load	0.05	0.1	0.65	0.020	0.021	13
Mixed/Active Load	25.05	0.1	0.65	0.016	6.6	8.2

Table 6.1: simulation values for two different cases

The small amount of resistance in the reactive load represents some active losses and it removes the DC-component in the output current.

This DC-component will appear in the beginning of the simulations due to that the simulations are performed without a current controller. The values for the capacitors are for the two-level inverter 2000uF, for the CMCI 10000uF and for the NPC 4000uF.

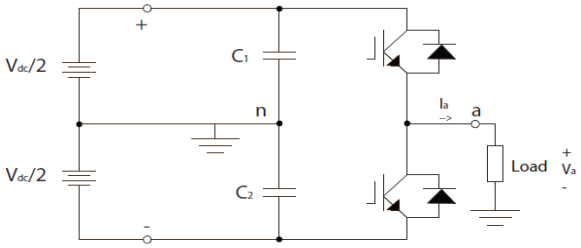


Fig 6.1: Two level simulation model

The inductance in the NPC balancing circuit is 0.01 H with a resistance of 0.1 Ohm.

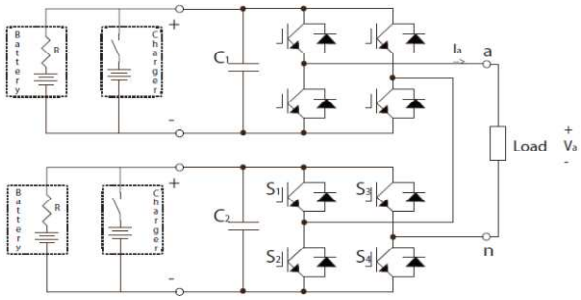


Fig 6.2: Five-level simulation model

These values were taken from the report [7] in which the balancing circuit was found since that also used the same value for the DC-capacitors.

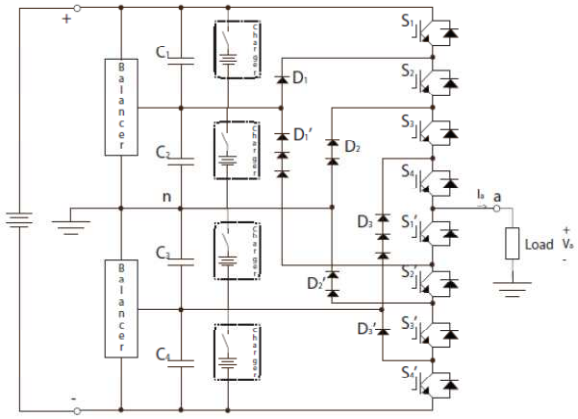


Fig 6.3: Five-level NPC simulation model

The switching frequency for the balancing circuit is 500 Hz. The current PI controller bandwidth was chosen to _i = 2_100 rad/s and the voltage PI controller bandwidth was chosen to _v = 2_20 rad/s.

VOLTAGE BALANCE FOR THE SELECTED MLIS VOLTAGE BALANCE FOR THE CASCADE MULTI CELL INVERTER (CMCI)

The Cascaded Multi cell Inverter (CMCI) with its use of several voltage sources is suitable in Electric Vehicles (EV) since battery cells is the power source. The battery cells may not always be equal and depending on the output demand the cells may be discharged unequally. It is therefore important to investigate the voltage source unbalance problem in the CMCI. In Figure 6.4 the results of the five-level CMCI connected to an active/mixed power load and a pure reactive power load can be seen. Each capacitor where charged to 500V during the beginning of the simulation with the charging voltage source, see Charger in Figure 6.2.

The charging voltage source where disconnected after the circuit reached steady-state operation. It should be noted that there are battery models connected to each module capacitor, recharging them over time so that they do not run out of stored energy. The battery models are rated to 500V with a resistance of 10 Ohm (see battery in Figure 6.2). The reason for the big battery resistance is that the sources should not be recharged to fast, so that the discharging and unbalance characteristics can be seen clearly. The modulation in the simulation was PSCPWM at 1050Hz switching frequency and the output voltage frequency was 50Hz. An odd multiple of the output voltage frequency is used for switching to eliminate output current offset, mainly for the pure reactive simulations.

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

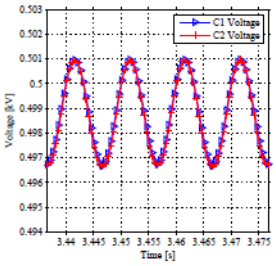


Fig 6.4 a) Reactive power transfer capacitor voltages

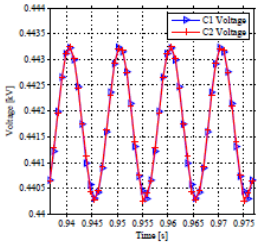


Fig 6.4 b) Active power transfer capacitor voltages

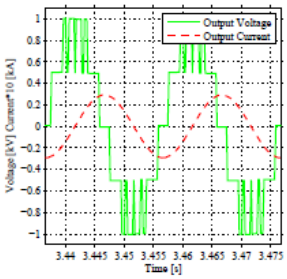


Fig 6.4 c) Reactive power transfer load voltage and current

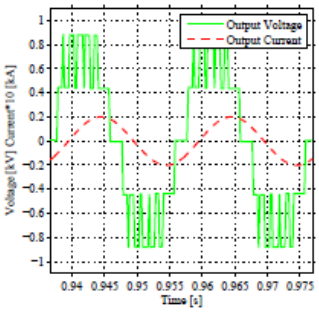


Fig 6.4 d) Active power transfer load voltage and current
Fig 6.4 a), b), c), d) is all unbalanced simulation

As can be seen in Figure 6.4 the voltages of the two capacitors C1 and C2 in the CMCI are balanced at steady normal operation. This is because that the PSCPWM discharges the sources equally, but it needs high switching frequency to do so. However, when the capacitors are charged with different magnitudes of voltage the voltages does not re-balance for any of the cases. In this work the voltage unbalance for the CMCI has been solved by adding the principle of voltage source prioritization, discussed earlier in Chapter 4. The modulation method uses m-1 = 4 carrier waves, two for positive voltage levels and two for negative voltage levels, like the PDPWM modulation in Subsection 3.2.2. Depending on what voltage source has the most charge the modulation compares the most prioritized inverter modules to the carriers closest to zero and those will hence be on during the longest time letting the less charged voltage sources catch. This also means that there is no injection of current for balancing the sources, which makes the method slow, especially for pure reactive power transfers. The results from active and reactive power transfers can be seen in Figure 6.5 for the five-level CMCI. Plot a) in Figure 6.5 shows the capacitors voltage after some time of operation for the pure reactive power transfer case. At this point the voltages are balanced but the duty priorities do not change. Due to the fact that the capacitors charge, while transferring only reactive power, does not change over one fundamental cycle. At the beginning of the simulation the capacitors where charged with different voltages, meaning that the higher charged module had the heaviest workload until a balanced state where reached. The beginning of the simulation is not seen in plot a) in Figure 6.5, see plot a) in Figure 6.6 where the capacitors are first unbalanced. The b) plot in Figure 6.5 is for active power transfer (active/mixed) where source capacitors where initially differently charged and it can be seen that the duty priorities change.

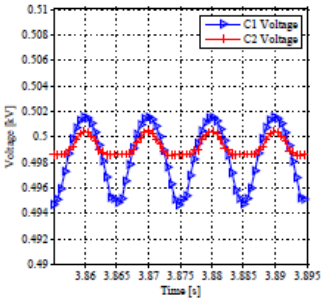


Fig 6.5 a) Reactive power transfer capacitor voltages

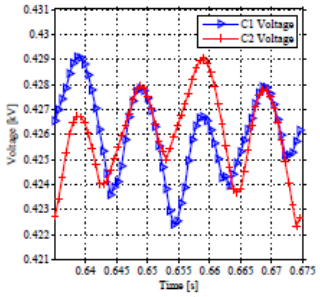


Fig 6.5 b) Active power transfer capacitor voltages

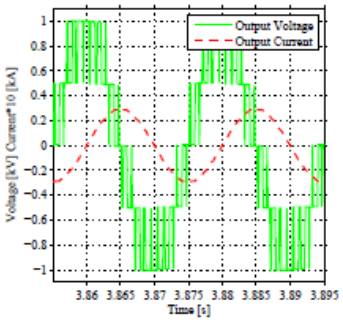


Fig 6.5 c) Reactive power transfer load voltage and current

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

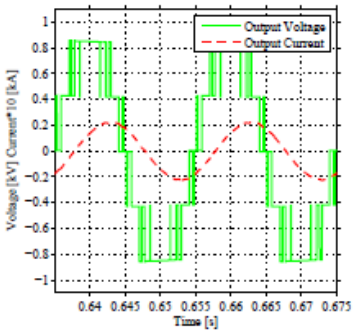


Fig 6.5 d) Active power transfer load voltage and current
Fig 6.5 a), b), c), d) is all balanced simulation

It can be seen that the priorities change since in the plot at about 0.64s and 0.66s the two capacitors have change workload with each other. The balancing prioritizing method effectiveness for both cases is clearly visible in Figure 6.6, where above plot shows the balancing response for the capacitors for the reactive power transfer case and below plot shows the voltage balancing response for active/mixed power transfer case. In plot a) it can be seen that for 0.25s the capacitor C1 is prioritized and is discharged more than capacitor C2, then the two capacitors are balanced to about the same voltage. Also in plot b) capacitor C1 is prioritized with heavier duty but only until about 0.1s. In between 0.1s and 0.12s it can be seen in plot b) that it is now capacitor C2 that has the heaviest duty since it is now discharged more than capacitor C1. Between 0.12s and 0.14s the prioritization changes back again. For the reactive case some of the balancing is because of that the battery is charging the capacitors.

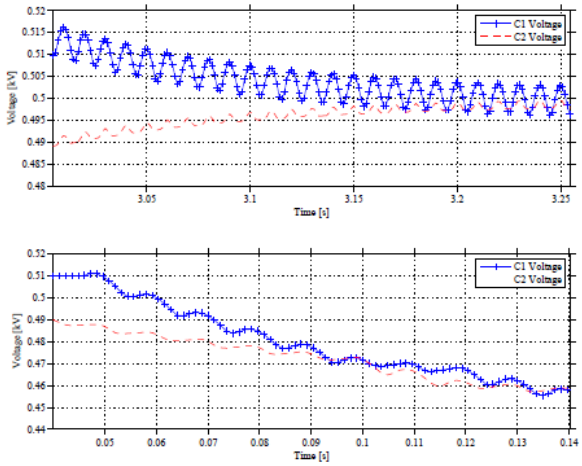


Fig 6.6 Capacitor balancing voltage responces for Reactive and Active powers

VOLTAGE BALANCE FOR THE NEUTRAL POINT CLAMPED INVERTER (NPCI)

As stated earlier NPCMLI has problem with balancing the capacitor voltage when transferring active power but it does not have this problem while only transferring reactive power. To show this, simulations with an active and a reactive load for the five-level NPC Inverter has been performed. During these simulations the DC-link capacitors where first charged to 500V with charging voltage sources to balance the capacitors voltages, see chargers in Figure 6.3. When the circuit reached steady-state the chargers where disconnected. Both cases were simulated using the PDPWM modulation method at 1050Hz switching frequency, see Subsection 3.2.2, and the fundamental output frequency was 50Hz. The reason for using an odd multiple of the output voltage frequency for switching was the same as for the CMCI simulation. The carrier waves where modulated with aspect of the current voltage magnitude for each respective voltage level.

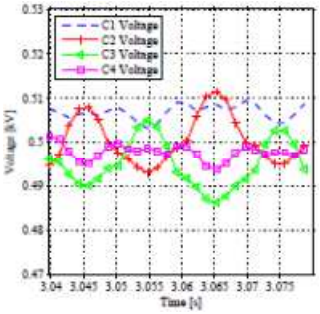


Fig 6.7 a) Reactive power transfer capacitor voltages

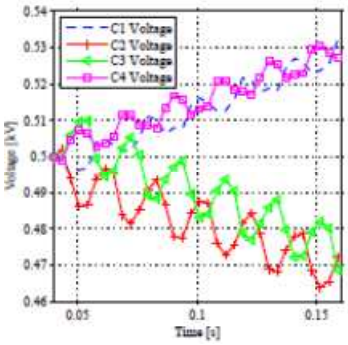


Fig 6.7 b) Active power transfer capacitor voltages

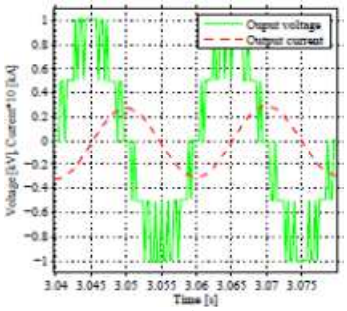


Fig 6.7 c) Reactive power transfer load voltage and current

In Figure 6.7 it can be seen how the voltages over the DC-link capacitors change for the two cases, active and reactive power transfer, for the five-level NPCMLI. The voltage in the plot a) is for the reactive power transfer case. As can be seen the voltages are not fixed, they vary periodically around 500V. Depending on what the current direction is when the charging voltage sources are disconnected it will differ if a capacitor is

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

charged or discharged first. In this case current is at lowest almost maximum

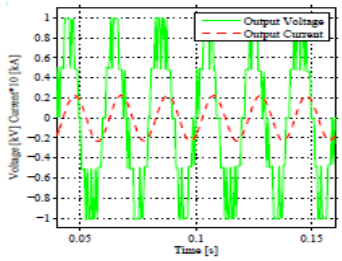


Fig 6.7 d) Active power transfer load voltage and current

Fig 6.7 a), b), c), d) is all Unbalanced simulation

negative magnitude when the charging voltage sources are disconnected. This leads to that C2 is initially charged, as can be seen in plot a). The range in which the voltages deviate depends on

How large the capacitors are. Figure 6.7, plot b), shows the capacitor voltages for when the five-level NPCMLI transfers active power. As can be seen the voltages oscillates in this case as well but the voltages unbalance is increasing with time. The reason for this lies in the charging of one capacitor and discharging of the other capacitor in the ±Vdc 4 voltage level, as discussed in section 2.1. In Figure 6.7 plot c) and d) the output voltages and current for the two cases can be seen. For the pure reactive case the capacitor voltages unbalance were also increasing over time since there were a small resistance in the load. To correct these voltage unbalances in the DC-capacitors additional balancing control is needed, either in the form of additional balancing modulation or additional balancing circuits. A balancing circuit found in [7], discussed in the chapter 4, was used in this

Work to simulate the balancing for the five-level NPC Inverter. By transferring energy between the capacitor pairs in the NPC five-level inverter the voltages could be held from deviating from each other.

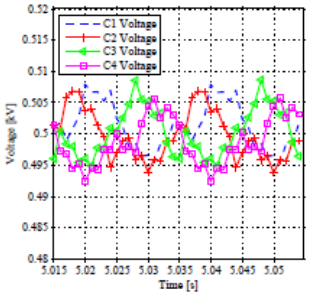


Fig 6.8 a) Reactive power transfer capacitor voltages

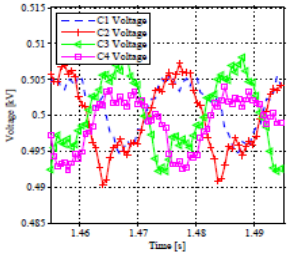


Fig 6.8 b) Active power transfer capacitor voltages

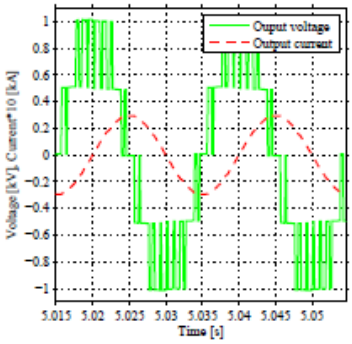


Fig 6.8 c) Reactive power transfer load voltage and current

In Figure 6.8 the DC-bus capacitors voltages for pure reactive power transfer, plot a), and active power transfer, plot b), can be seen. In plot a) the capacitor voltages do vary around 500V but get more balanced over time, as can be seen in Figure 6.9 above plot, and hence vary with lower magnitude.

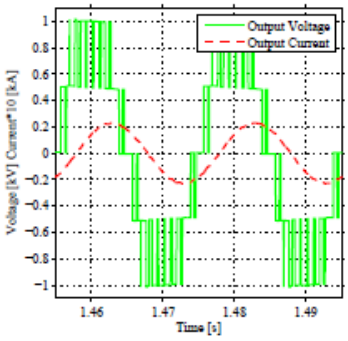


Fig 6.8 d) Active power transfer load voltage and current

Fig 6.8 a), b), c), d) is all balanced simulation

The voltage varies since the capacitors are still charged and discharged by the reactive power transferred.

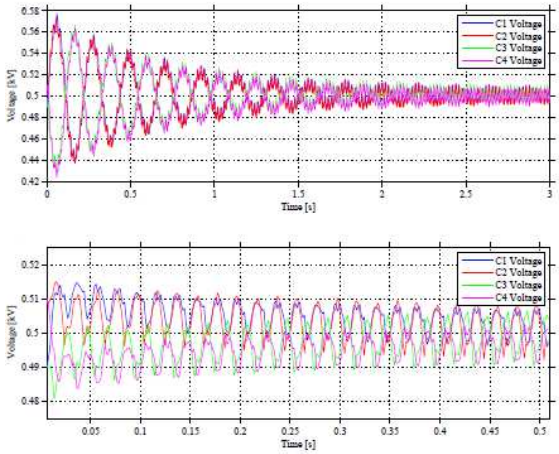


Fig 6.9 Capacitor balancing voltage responses for Reactive and Active powers

below plot show the results from the active power simulation and compared to the unbalanced case the capacitor voltages does no longer get unbalanced over time but are held balanced by the balancing circuit, even though there are some oscillations. The oscillations come from that the circuit

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 1, January 2015)

transfers both active and reactive power, so there is some charging involved in the process. Also, another reason for the oscillations, or rather why the balancing circuit cannot control these variations as well, is that the voltage controller is to slow for these oscillations. As stated, the voltage controller bandwidth is 20Hz and the oscillations have a frequency of 50Hz, making the controller unable to remove these oscillations. The balancing circuit is also implementable on NPC inverters switched with fundamental switching frequency with similar results. The voltage balancing response for the active power transfer simulation can be seen in Figure 6.9 b). The output voltages and currents for the reactive and active power simulations can be seen in Figure 6.8 c) and d).

CONCLUSION

This paper presented several topologies for multilevel inverters (MLI), some of them well known with applications on the market. Every topology has been described in detail. Several modulation techniques have also been presented which are to be used with the presented topologies. Topology comparisons, such as number if components and their ratings, have been presented and shows that multilevel inverters compete with two-level inverters in the

Area of voltage ratings for their components (diodes, switches and such), even though the number of components needed for multilevel inverters, as shown, can be very high. For a five-level MLI case the voltage rating requirements is only one fourth of that of the two level inverter, but four times more switches are needed (for components with different ratings).

The simulation results concerning both the discussed voltage balancing problem and comparison with a two-level inverter for the Cascade Multi cell inverter (CMCI) and the Neutral-Point Clamped (NPC) inverter. For the balancing problem it is shown with simulation results that the voltage levels, with different strategies, can be balanced for both the CMCI and the NPC inverter. For the NPC inverter an additional balancing circuit was used that with both active and reactive power load could balance the voltages in the DC-bus capacitors, with a variation of about ±1% in both cases. For the CMCI a modulation strategy that prioritized modules depending on stored charge, showed that the voltage levels in this inverter could be

Discharged equally. Especially for the active power load where a voltage difference of 20V, while transferring 6.6 kW, where balanced in 0.1 seconds. Since balancing solutions where presented for both simulated topologies in this paper, the possibility has been shown to use multilevel inverter with potential methods of treating the problem of voltage unbalance.

The multilevel topologies have also been tested in several simulations and compared with the two-level inverter presented in this paper.

REFERENCES

[1] N. G. Hingorani and L. Gyugyi, "Understanding FACTS" , IEEE Press, 2000

[2] Rodriguez, J.; Jih-Sheng Lai; Fang Zheng Peng; , "Multilevel inverters: a survey of topologies, controls, and applications," Industrial Electronics, IEEE Transactions on , vol.49, no.4, pp. 724- 738, Aug 2002 doi: 10.1109/TIE.2002.801052

[3] Jih-Sheng Lai; Fang Zheng Peng; "Multilevel converters-a new breed of power converters," Industry Applications, IEEE Transactions on , vol.32, no.3, pp.509- 517, May/Jun 1996 doi: 10.1109/28.502161

[4] Panagis, P.; Stergiopoulos, F.; Marabeas, P.; Manias, S.; , "Comparison of state of the art multilevel inverters," Power Electronics Specialists Conference, 2008. PESC 2008. IEEE , vol., no., pp.4296-4301, 15-19 June 2008 doi:10.1109/PESC.2008.4592633

[5] Hemant Joshi, P. N. Tekwani, Amar Hinduja, Implementation of a Five- Level Inverter Using Reversing Voltage Topology: A Competitive Solution for High- Power IM Drive Application. Indian Institute of Technology Roorkee.

[6] McGrath, B.P.; Holmes, D.G.; , "Multicarrier PWM strategies for multilevel inverters," Industrial Electronics, IEEE Transactions on , vol.49, no.4, pp. 858- 867, Aug 2002 doi: 10.1109/TIE.2002.801073

[7] Newton, C.; Sumner, M.; , "Novel technique for maintaining balanced internal DC link voltages in diode clamped _ve-level inverters," Electric Power Applications, IEE Proceedings - , vol.146, no.3, pp.341-349, May 1999 doi: 10.1049/ip-epa:19990103

[8] Siemaszko, D.; Antonopoulos, A.; Ilves, K.; Vasiladiotis, M.; Ängquist, L.; Nee,H.-P.; , "Evaluation of control and modulation methods for modular multilevel converters," Power Electronics Conference (IPEC), 2010 International , vol., no pp.746-753, 21-24 June 2010 doi: 10.1109/IPEC.2010.5544609

[9] N. Mohan, T. Undeland, and W. Robbins, _Power Electronics: Converters, Applications, and Design_, Wiley, 2003, ISBN:978-0-471-22693-2