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High Performance and Power Efficient 32-bit Carry Select Adder using Hybrid PTL/CMOS Logic Style

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Abstract: **- Highly-increasing requirement for mobile and several electronic devices want the use of VLSI circuits which are highly power efficient. The most primitive arithmetic operation in processors is addition and the adder is the most highly used arithmetic component of the processor. Carry Select Adder (CSA) is one of the fastest adders and the structure of the CSA shows that there is a possibility for increasing its efficiency by reducing the power dissipation and area in the CSA. This research paper presents power and delay analysis of various adders and proposed a 32-bit CSA that is implemented using Hybrid PTL/CMOS logic style. This work evaluates and analyses the performance of the proposed designs in terms of area, delay, power. The results analysis is showing that the proposed CSA structure shows better result in terms of area, power and PDP (Power Delay Product) than the others.**

Keywords: **CMOS logic, adder, Hybrid PTL, Carry Select Adder, CSA structure.**

1. INTRODUCTION

In recent years, the increasing demand for high-speed and blow power arithmetic units in floating point co-processors, image processing units and DSP chips has resulted in the development of high-speed adders, as addition is an obligatory and mandatory function in these units. A compact and a high performance adder play an important role in most of the hardware circuits. Adders are used in microprocessor system based application for arithmetic addition and for computation in large electronics circuit. Less efficient and low power adders would lead to an increase in the total power dissipation in the circuit and delay as well, so processing in these devices is required to be accomplished by making use of low-power; area-efficient circuits processing at a higher speed. On the basis of requirements such as area, delay and power consumption, different types of adder, such as ripple carry, carry-skip and carry look-ahead are present in the literature [1-7]. Ripple carry adders shows the most compact design but slowest in speed, whereas carry look-ahead adder is the fastest one but it consumes more area. On the other hand, carry select adders act as a compromise between the two adders because it reduces the problem of carry propagation delay. However, the CSA generates partial sum and carry by using multiple pairs of Ripple Carry Adders (RCA) so it requires large area. CMOS circuits are most commonly used building blocks in digital integrated circuits. One of the major concerns in VLSI design is power consumption. Power consumption has become an important factor due to continuous decline in size of CMOS circuits and increase in chip density and frequency at which circuits are operating. Logic styles used in a particular logic circuit affect various parameters such as power dissipation, operating speed, size and wiring complexity of those logic circuits [2], [3]. Pass Transistor Logic (PTL) logic styles that have been developed in recent times are more efficient and exhibit better results, in comparison with traditional CMOS logic for some designs of arithmetic unit. In terms of power dissipation, delay and area PTL and CMOS logic have their respective advantages and disadvantages, so at the circuit level, by combining PTL with static CMOS logic that is Hybrid PTL/CMOS logic very low power dissipation, low power delay product and less area can
be achieved in the circuit. Amount of power saved in Hybrid PTL/CMOS logic circuit is more than 60 percent as compared to conventional static CMOS logic circuit. [2] This paper presents a comparative analysis of various adders and proposed design of a new 32 bit carry select adder by sharing common Boolean logic term using Hybrid
PTL/CMOS logic style, which shows least power dissipation and PDP than other adders with less transistor count. This brief is structured as follows. Section II surveys various digital adders. Section III presents Hybrid PTL/CMOS
logic style. The proposed CSA using Hybrid PTL/CMOS logic presented in Sections IV. The simulation results are
analyzed in Section V. Finally, the work is concluded in Section VI.

Disadvantages of Existing Work:

The carry select adder design requires more number gates. But it is better to the adder circuits was designed with basic logic. But this carry select adder having more gates it will cause the area and gate delay to the adder circuit. This will gives low throughput to adder circuit while doing computing operations and also this circuit will take more area.

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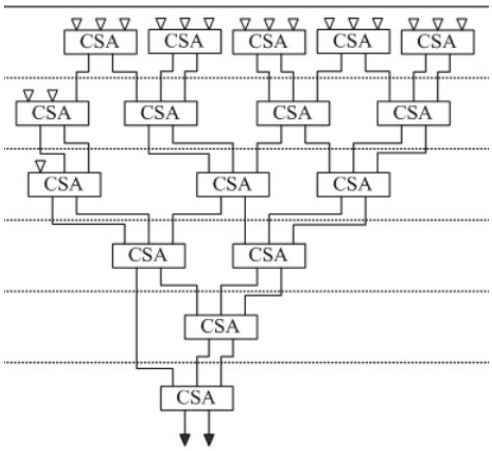
2. PROPOSED WORK

Highly-increasing requirement for mobile and several electronic devices want the use of VLSI circuits which are highly power efficient. The most primitive arithmetic operation in processors is addition and the adder is the most highly used arithmetic component of the processor. In this research work to reduce the gate count and gate delay we are designing a Wallace tree structure based adder with more bit compressor technique. The Wallace tree structure will provide to the high speed while doing computation task.

Advantages of Proposed Work:

Less number of gate usage, reduced area and faster operations at computational task, and also this work will provide high throughput while doing computational task.

3. WALLACE TREE STRUCTURE ADDER



The overall System Architecture will be designed using HDL language and simulation, synthesis and FPGA implementation (Translation, Mapping, Placing and Routing) will be done using various FPGA based EDA Tools.

4. VLSI EDA TOOLS

Xilinx ISE: Integrated Software Environment (ISE) enables to quickly Design, Simulation of HDL source, Synthesis of HDL based RTL design and FPGA Implementation (Placing, routing ,mapping) and Bit Stream generation.

5. CONCLUSION

In VLSI design, power and area are the constituent factors which limit the performance of any circuit. High Performance and power efficient circuits can be designed using Hybrid PTL/CMOS logic style. Hence 32 bit CSA using Hybrid PTL/CMOS logic style has been proposed. It has been found that the transistor count, power dissipation of the improved adder using Hybrid PTL/CMOS logic style is less than that of other conventional designs .The comparisons of adder design are based upon Predictive Model Beta Version 90nm CMOS technology in tanner EDA tool.

REFERENCES

[1]. I-chyn Wey, Cheng Chen Ho, Yi-Sheng Lin ,and Chien- Chang Peng "An Area Efficient Carry Select adder design by sharing the Boolean Logic term"vol-II,IMECS 2012,March 14- 16 2012,Hong Kong.
[2]. O.Bedrij,"Carry Select Adder",IRE trans on Electronic Computers Vol EC-II,pp 340-346.1962.
[3]. JM Rabaey,"Digital Integrated Circuits",IEEE trans on VLSI SYSTEMS 2003.
[4]. Shen Fu Hsiao,Member,IEEE,Mingyu Tsai, and Chia ShengWen "Circuits and Systems-II";Expres Briefs ,Vol 57,No1 January 2010.
[5]. B. Ramkumar and Hrish M kittur, "Low-Power and Area Efficient Carry Select Adder" in IEEE transaction on Very Large Scale Integration (VLSI) Systems, Vol.20, No.2, February 2012.
[6]. Padma Devi, Ashima Girdhar, Balwinder Singh, "Improved Carry Select Adder with Reduced Area and Low Power Consumption"in International Journal of Computer Applications, Vol.3, No.4, June 2010.
[7]. B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.
[8]. Geetanjali Sharma, Uma Nirmal, Yogesh Mishra, "Comparative Analysis of High Performance Full Subtractor using Hybrid PTL/CMOS Logic" in proceeding of International Conference on Advances in Information Communication Technology and VLSI Design, Coimbatore, India, August 2010.
[9]. Geetanjali Sharma, Uma Nirmal, Yogesh Mishra, "Synthesis of Hybrid PTL/CMOS Logic for Low Area/Power Applications" in proceeding of International Conference on System Dynamics and Control, India, August 2010.
[10]. Shen-Fu Hsiao Ming-Yu Tsai, and Chia-Sheng Wen,"Low Area/Power Synthesis using Hybrid Pass Transistor/CMOS Logic Cells in Standard Cell-based Design Environment," IEEE Trans. Circuits and Systems vol. 57, NO.1, Jan 2010.
[11]. G. R. Cho and T. Chen, "Synthesis of Single/Dual-Rail Mixed PTL/Static Logic for Low-Power Applications," IEEE Trans. Computer-Aided Design Integration Circuits Syst., vol.23, no. 2, pp. 229–242, Feb. 2004.