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# A Novel Architecture for High Latency BIST using Window Vectors and SRAM Cells

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***Abstract:*** **Input vector monitoring concurrent built-in self test (BIST) schemes perform testing during the normal operation of the circuit without imposing a need to set the circuit offline to perform the test. These schemes are evaluated based on the hardware overhead and the concurrent test latency (CTL), i.e., the time required for the test to complete, whereas the circuit operates normally. In this brief, we present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff.**

***Keywords:*** **comparator, test generator enable, concurrent BIST unit, modified SRAM, logic module, concurrent test, response verifier**

## 1. INTRODUCTION

Built-in self test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage, whereas simultaneously they relax the reliance on expensive external testing equipment. Hence, they constitute an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into offline and online.

Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV). Therefore, to perform the test, the normal operation of the CUT is stalled and, consequently, the performance of the system in which the circuit is included, is degraded.

**1.1.** ***Input Vector Monitoring Concurrent BIST:*** Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT; if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig. 1. The CUT has n inputs and m outputs and is tested exhaustively; hence, the test set size is N = 2n. The technique can operate in either normal or test mode, depending on the value of the signal labeled T/N. During normal mode, the vector that drives the inputs of the CUT (denoted by d[n:1]) is driven from the normal input vector (A[n:1]). A is also driven to a concurrent BIST unit (CBU), where it is compared with the active test set. If it is found that A matches one of the vectors in the active test set, we say that a hit has occurred. In this case, A is removed from the active test set and the signal response verifier enable (rve) is issued, to enable the m-stage RV to capture the CUT response to the input vector [1]. When all input vectors have performed hit, the contents of RV are examined. During test mode, the inputs to the CUT are driven from the CBU outputs denoted TG[n:1]. The concurrent test latency (CTL) of an input vector monitoring scheme is the mean time (counted either in number of clock cycles or time units) required to complete the test while the CUT operates in normal mode.

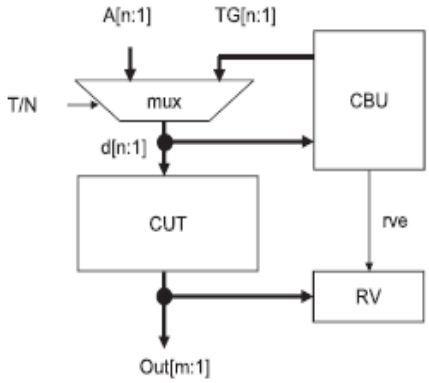


Fig. 1. Input vector monitoring concurrent BIST

Above figure indicates that Input vector monitoring concurrent BIST. In this brief, a novel input vector monitoring concurrent BIST scheme is proposed, which compares favorably to previously proposed schemes with respect to the hardware overhead/CTL tradeoff.

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## 2. ARCHITECTURE

***a) Hardware test pattern generator***: This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs. As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG algorithms on the CUT Using the hardware test pattern generator is not feasible. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2n-1, if there are n flip-flops in the register) as possible.

***b) Decoder:*** A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2n , binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. Decoding is necessary in applications such as data multiplexing, 7 segment display. The example decoder circuit would be an AND gate because the output of an AND gate is "High" (1) only when all its inputs are "High." Such output is called as "active High output". If instead of AND gate, the NAND gate is connected the output will be "Low" (0) only when all its inputs are "High". Such output is called as "active low output". A slightly more complex decoder would be the n-to-2n type binary decoders. These type of decoders are combinational circuits that convert binary information from 'n' coded inputs to a maximum of 2n unique outputs, the decoder may have less than 2n outputs. There is 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder.

**c*) Comparator:*** is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The circuit, for comparing two n-Bit numbers, has 2n inputs. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary from one logic style to another and thus proper choice of logic style is important. The test generator value from the logic block and the higher order bits from the mux unit are compared and the output is given to the logic module block from which the output is obtained based on testing. The testing process is carried out in parallel manner. Based on which the response verifier is activated.

***d) SRAM***: SRAM is a type of semiconductor memory that uses bitable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data eminence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used with applications such as moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption in the region of a few micro-watts.

***e) CUT:*** During normal mode, the inputs to the CUT are driven from the normal inputs. The n inputs are also driven to the CBU as follows: the w low-order inputs are driven to the inputs of the decoder; the K high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (clk and cmp are enabled) the addressed cell is read; because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop enables the AND gate (other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.

***f) Mux:*** Mux serve as the examples for circuit analysis and modular design. A -to-1 multiplexer sends one of input lines to a single output line. A multiplexer has two sets of inputs: data input lines .n select lines, to pick on the data inputs The mux output is a single bit which is one of the 2n data inputs.

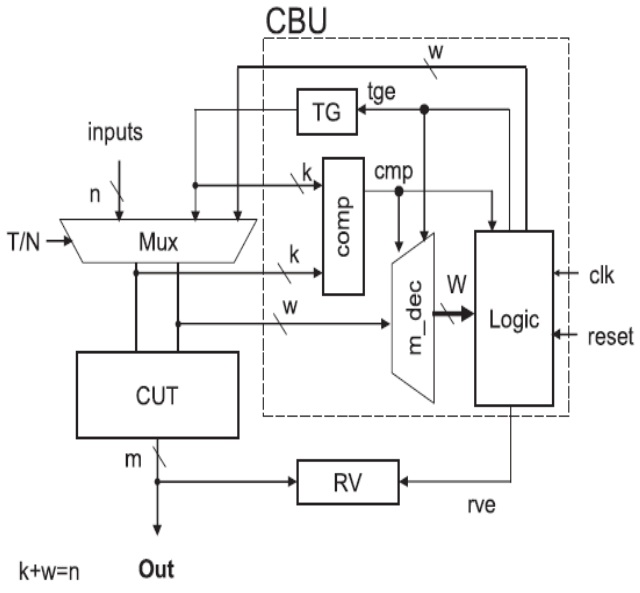


Fig. 2. Architecture.

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## 3. PROPOSED SCHEME

Let us consider a combinational CUT with *n* input lines, as shown in Fig. 2; hence the possible input vectors for this CUT are 2*n*. The proposed scheme is based on the idea of monitoring a window of vectors, whose size is *W*, with *W* = 2*w*, where *w* is an integer number *w* < *n*. Every moment, the test vectors belonging to the window are monitored, and if a vector performs a hit, the RV is enabled.

The bits of the input vector are separated into two distinct sets comprising *w* and *k* bits, respectively, such that *w* + *k* = *n*. The *k* (high order) bits of the input vector show whether the input vector belongs to the window under consideration. The *w* remaining bits show the relative location of the incoming vector in the current window. If the incoming vector belongs to the current window and has not been received during the examination of the current window, we say that the vector has performed a hit and the RV is clocked to capture the CUT's response to the vector. When all vectors that belong to the current window have reached the CUT inputs, we proceed to examine the next window.

The module implementing the idea is shown in above Figure. It operates in one out of two modes, normal, and test, depending on the value of the signal T/N. When T/N = 0 (normal mode) the inputs to the CUT are driven by the normal input vector. The inputs of the CUT are also driven to the CBU as follows: the k (high order) bits are driven to the inputs of a k-stage comparator; the other inputs of the comparator are driven by the outputs of a k-stage test generator TG. The proposed scheme uses a modified decoder (denoted as m) and a logic module based on a static-RAM (SRAM)-like cell, as will be explained shortly.

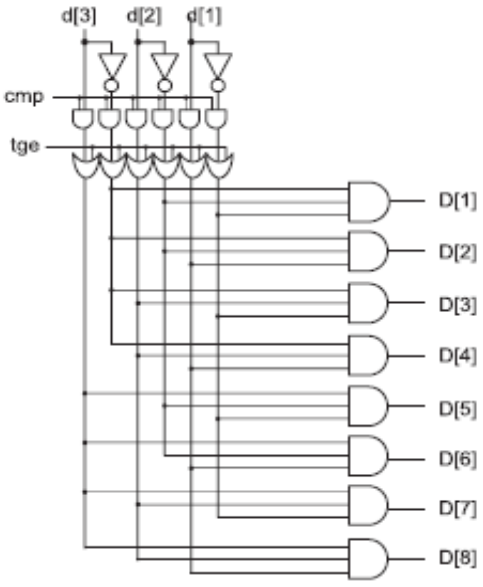


Fig. 3. Modified decoder design used in the proposed architecture

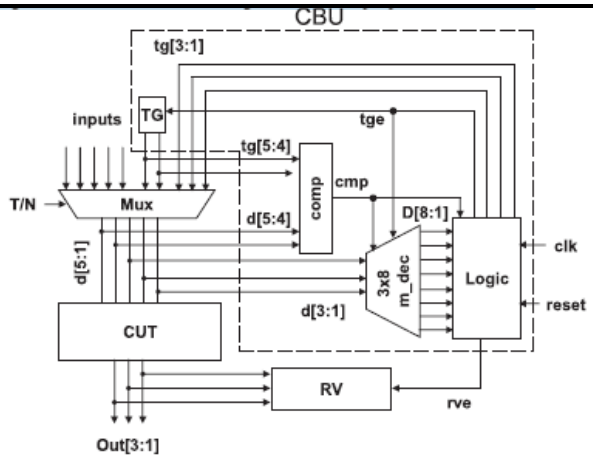


Fig.4. Proposed architecture for *n* = 5, *w* = 3, and *k* = 2

The design of the m_dec module for *w* = 3 is shown in Fig. 3 and operates as follows. When test generator enable (tge) is enabled, all outputs of the decoder are equal to one. When comparator (cmp) is disabled (and tge is not enabled) all outputs are disabled. When tge is disabled and cmp is enabled, the module operates as a normal decoding structure.

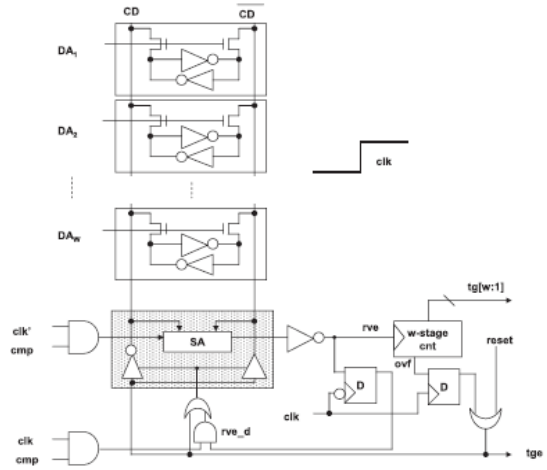


Fig.5. Design of the logic module

The architecture of the proposed scheme for the specific case n = 5, k = 2, and w = 3, The module labeled logic in comprises W cells (operating in a fashion similar to the SRAM cell), a sense amplifier, two D flip-flops, and a w-stage counter (where w = log2W). The overflow signal of the counter drives the tge signal through a unit flip-flop delay. The signals clk_ and clock (clk) are enabled during the active low and high of the clock, respectively.

In the sequel, we describe the operation of the logic module, presenting the following cases: 1) reset of the module; 2) hit of a vector (i.e., a vector belongs in the active window and reaches then CUT inputs for the first time); 3) a vector that belongs in the current window reaches the CUT inputs but not for the first time; and 4) tge operation (i.e., all cells of the window are filled and we will proceed to examine the next window).

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## 4. SIMULATION RESULTS

In the Input vector monitoring concurrent bist architecture the simulation results are shown below. In figure 6 represents the normal mode with reset 0 condition then the outputs are 3bit count from 0 to 3 and 7 to 4 and response verifier output is with negative edge delay shown here.

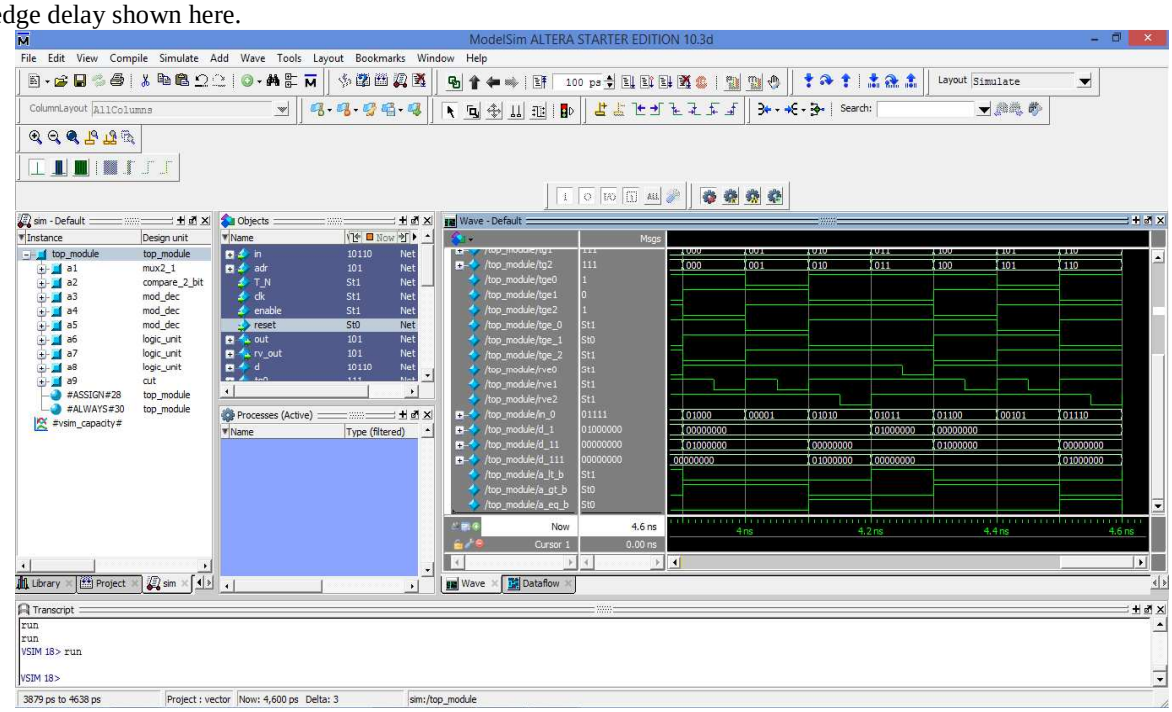


Fig.6. Input vector monitoring concurrent bist with normal mode when reset zero.

In figure 6 represents the normal mode with reset 1 condition then the outputs are 3bit count from 0 to 3 and 7 to 4 and response verifier output is with negative edge delay shown here.

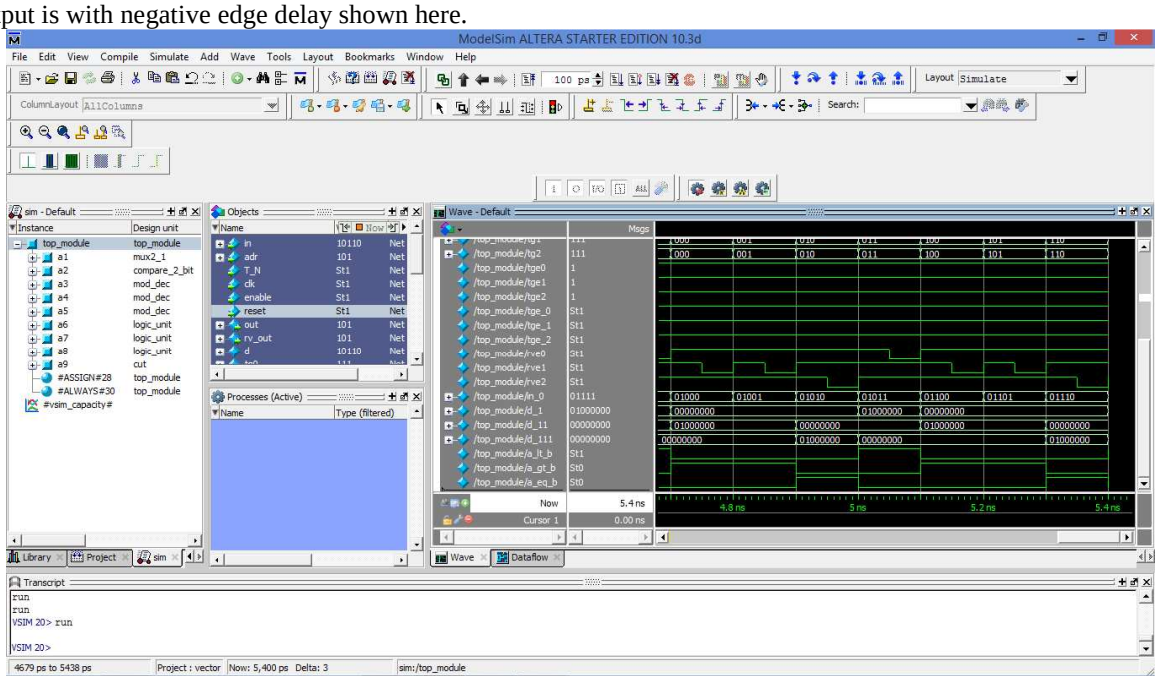


Fig.7. Input vector monitoring concurrent bist with normal mode when reset one.

In figure 8 represents the test mode with reset 1 condition then the outputs are 3bit count from 0 to 3 and 7 to 4 and response verifier output is with negative edge delay shown here. And the different input vectors are generated for the monitoring.

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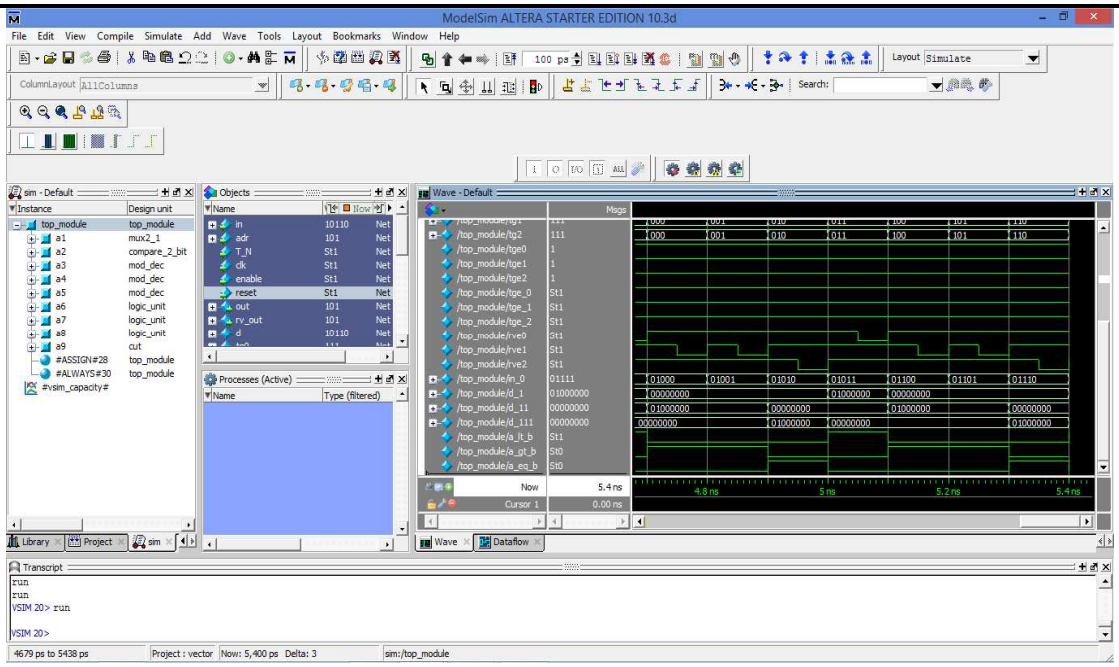


Fig.8. Input vector monitoring concurrent bist with test mode.

## 5. CONCLUSION

BIST schemes constitute an attractive solution to the problem of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can circumvent problems appearing in offline BIST techniques.

### Advantages

- BIST has an advantage over cost and memory storage reduction.
- BIST eliminates the necessity of high-bandwidth test interactions and allows at-speed testing.
- Other benefits of BIST include reduced product development cycle and cost-effective system maintenance.

### Applications

- In most of the embedded system applications, real time computing is used. The operations execute within the strict constraints called system deadlines.
- The anti-lock brakes on a car are a simple example of a real-time computing system.
- The controllers that manage anti-lock brakes must continue to perform its intended real-time function during its entire lifetime.
- The controllers which are very large scale integration (VLSI) circuits can become faulty in the due course of their operation. Some faults that arise later in the lifetime, because of electro-migration, stress, time-dependant dielectric breakdown or thermal cycling, make estimation of mean-time-to-failure (MTTF) very difficult at design time and consequently, failure detection at runtime.

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