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FPGA Implementation of Low Logical Cost Conservative Reversible Adders using Novel PCTG

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***Abstract* — Reversible Logic is one of the emerging computing technologies which assures zero power dissipation theoretically Through thermodynamically proven principles. Its applications cover a wide spectrum starting with Low Power VLSI, quantum computing, Bio Informatics, Optical Circuits to Nanotechnology based systems. It can take in hand the issues of Fault tolerance through a special class of gates called parity conserving reversible logic gates. This paper aims to study the design a fault tolerant full adders using the new Parity Conserving Toffoli Gate, which is in turn employed to construct ripple carry adders, and high speed adders like carry skip adder. The design has the most optimized performance parameters in terms of Logical Cost than its counterparts in the literature.**

***Keywords* - Reversible Logic Gates, PCTG, Total Logical Cost, Fault Tolerant Full Adder, Quantum Computing.**

I. INTRODUCTION

It has been shown by Landauer [1] that every bit of information lost will generate kTlog2 joules of energy k is Boltzmann's constant and T is absolute temperature at which computation is performed. Later it was shown by Bennett [2] that this energy dissipation would not occur, if a computation is carried out in a reversible way. Reversible computing is motivated by the Von Neumann Landauer (VNL) principle, a theorem of modern physics which states that ordinary irreversible logic operations which destructively overwrite previous outputs incur a fundamental minimum energy cost. Such operations typically dissipate roughly the logic signal energy, itself irreducible due to thermal noise. This fact threatens to end improvements in practical computer performance within the next few decades. However, computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach arbitrarily near to 100% as the quality of the hardware is improved, reopening the door to arbitrarily high computer performance at a given level of power dissipation.

The primary motivation for reversible computing lies in the fact that it provides the only way (that is, the only way that is logically consistent with the most firmly-established principles of fundamental physics) that performance on most applications within realistic power constraints might still continue increasing indefinitely. The parity conserving reversible logic gates are one class of reversible logic gates that have unique property of fault tolerance derived from parity conservation techniques which can be efficiently used to design fault tolerant arithmetic circuits.

In this paper we study the new structure for the fault tolerant full adder using the Parity Conserving Toffoli gate, which has been used to design ripple carry adders and carry skip adder. The remainder of the paper is organized as follows:

Section II gives the terminologies pertaining to the reversible logic and explains some of the basic as well as parity preserving reversible logic gates. Section III gives the design of the proposed adder whose design is used in ripple carry adder and carry skip adder. Section IV gives the analyses and comparisons of different performance parameters.

II. REVERSIBLE LOGIC

A. *Terminologies:*

Some of the basic definitions [10] pertaining to reversible logic are mentioned below. *Reversible Logic Function* is a Boolean Function f(x1, x2, x3,….xN) that satisfies the following criteria : (i)The number of inputs is equal to the number of the number of utputs.(ii)Every output vector has an unique preimage. *Reversible Logic Gate* is an N-input N-output logic device that provides one to one mapping between the input and the output. *Garbage Outputs (GO)* are the additional outputs can be added so as to make the number of inputs and outputs equal whenever necessary. The number of outputs which are not used in the synthesis of a given function are called garbage outputs. *Quantum Cost (QC)* refers to the cost of the circuit in terms of the cost of a primitive gate and is computed knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. *Gate levels or Logic Depth* refers to the number of levels in the circuit which are required to realize the given logic functions. *Flexibility* refers to the universality of a reversible logic gate in realizing more functions.

Gate count (GC) – The number of reversible gates used to realize the function. *Constant*
Inputs (CI) refer to the number of inputs that are to be maintained constant (either at 0 or 1) in order to synthesize a given logic function.

Total Logical Cost – This is measured by
counting the number of AND operations, number of EX-OR operations and number of NOT operations. Let α = No. of EXOR operations β = No. of AND operations δ = No. of NOT

operations then the total logical cost T is given as sum of number of AND, EX-OR and NOT operation.
The Vedic mathematics mainly reduces the complex typical calculations in to simpler by applying sutras as stated above. These Vedic mathematic techniques are very efficient and take very less hardware to implement. These sutras are mainly used for multiplication of two decimal numbers and we extend these sutras for binary multiplications. Some of the techniques are discussed below.
T= N (α).α+ N (β).β+ N (δ).δ (1)
Where N (*) denotes "number of"
Total Reversible Logic Implementation Cost (TRLIC): Thisparameter [11] is defined as the sum of all the cost metrics of a reversible logic circuit viz,. the CI, GC, QC and GO. The TRLIC is a parameter which reflects the overall performance of a reversible logic circuit. TRLIC=Σ (CI, GC, QC, GO) (2)

B. *Basic Reversible Logic Gates*

The basic reversible logic gates that are widely studied in the reversible logic are:
1) Feynman Gate:
It is a 2x2 gate with quantum cost of one. It is also called Controlled NOT (CNOT) gate depicting its operation;
the gate and its reversible logic circuit [5] are as shown in Fig.1.
2) Peres Gate:
It is a 3x3 gate [3] that has input output combination as (A→ P = A, B→ Q = A⊕B, C→ R = AB⊕C). It is a 3x3 gate with a quantum cost of 4.
3) Fredkin Gate:
It is also a 3x3 gate [4] which maps inputs (A, B, C) to output (A, A'B+AC, A'C+AB). It has a quantum cost of five and is a parity preserving gate as well as a universal gate.
4) Toffoli Gate:
It is a 3x3 gate [4] with input output mapping given by (A→ P = A, B→ Q = B, C→ R= AB⊕C). It has a quantum cost of five and is also a universal gate. Its gate diagram and
quantum circuit are as shown in the fig 1.

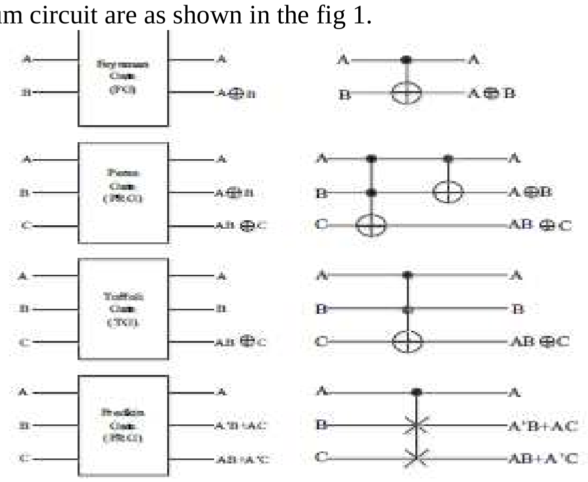

FIGURE 1: BASIC REVERSIBLE LOGIC GATES

Figure 1: Basic Reversible Logic Gates

C. *Parity preserving Reversible Logic Gates*

A reversible logic gate will be parity preserving if the EXOR of the inputs matches the EX-OR of the outputs i.e., parity of the input and the output remains the same. If I1, I2,. , IN and O1, O2,…, ON are the inputs and outputs of an NxN reversible logic gate, it will be parity preserving if they satisfy. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving. Some of the parity preserving reversible
logic gates is as follows:

1) Double Feynman Gate:
It is a cascade of two Feynman gates and is the simplest among all. The inputs I (A, B, C) are mapped to outputs O (A, A⊕B, A⊕C). It has a quantum cost of two [6]. The gate is as shown in Fig. 2.

2) NFT Gate:
It is a 3x3 gate that has input output relation given by (A→ P = A⊕B, B→ Q = BC'⊕AC', C→R = BC⊕AC') [12].
It has a quantum cost of five and the gate diagram is as depicted in Fig. 2.

3) Our Proposed Parity Conserving Toffoli Gate (PCTG):
Toffoli is one of the universal gates as well as a self reversible gate i.e. the gate is same as its dual. The dual of a gate is an inverse that reverses its logic function. PCTG [20] is
parity preserving version of Toffoli Gate. This gate has a quantum cost of 7 and the reversible implementation is as shown in Fig. 2.

4) Islam Gate (IG), F2PG and PPPG:
It is a 4x4 gate [8] that has a quantum cost of 7. F2PG is a 5x5 gate whose quantum cost has not been specified by [13]. PPPG is also a 5x5 gate [7] and it quantum cost is unspecified. Single F2PG and PPPG gate can be used as a Full Adder

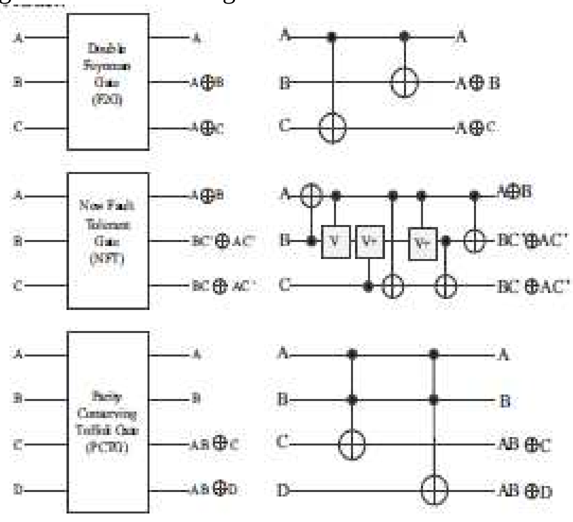

FIGURE 2: PARITY PRESERVING REVERSIBLE LOGIC GATES

Figure 2: Parity Preserving Reversible Logic Gates

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III. PCTG AND PARITY PRESERVING ADDER DESIGNS

Full Adder is one of the most basic and versatile components of most of the arithmetic circuits like the Carry Save adder, Ripple Carry adder, BCD Adder, and even most complex Arithmetic Logic Units. Thus fault tolerant implementation of this full adder structure is basic requisite. There are innumerous attempts in the literature to build full adders using reversible logic gates out of which only handful of them are fault tolerant. Some noteworthy works in this area are enlisted in the next few lines of this section. A full adder is generally designed using a Toffoli gate. The Toffoli being a non conservative gate, the other parity preserving reversible logic gates are used to design a Parity Preserving Toffoli structure. One such implementation where two Double Feynman and one Fredkin gates are used has been proposed in [17]. The Total Logical Cost of this Toffoli is T=6α+4β+2δ and the quantum cost is 9. In [12] another such implementation is encountered where the design consists of a NFT and a Double Feynman gate, with Hardware complexity and quantum cost as T=5α+3β+2δ and 7. [18] has also proposed a fault Tolerant Toffoli gate which uses a Fredkin and a Double Feynman gate with T=4α+4β+2δ and quantum cost of 7. The proposed Parity Conserving Toffoli Gate (PCTG) can directly be modified to produce Toffoli functionality. These Parity Preserving Toffoli gates are cascaded along with Double Feynman gates in order to obtain a Fault Tolerant Full Adder Structure [16] shown in fig 4.

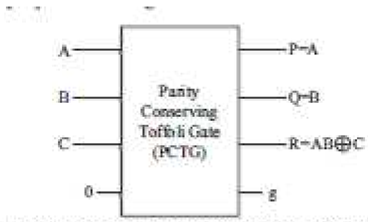

FIGURE 3: PROPOSED PARITY CONSERVING TOFFOLI STRUCTURE

Figure 3: Proposed Parity Conserving Toffoli Structure

The above four mentioned designs can be substituted in the structure shown in [16] so as to obtain a Fault Tolerant Full Adder (FTFA). [18] has also proposed the IG which can be cascaded to obtain a parity preserving Full adder. [19] has also proposed a Fault Tolerant Full adder which makes use of three Double Feynman gates and one NFT gate. [15] has proposed a FTFA using four Fredkin gates. In [7] and [13] a single gate has been designed that functions as FTFA by setting two of its inputs at constant values i.e., at binary zero. The ripple carry adder is obtained by series connecting the FTFAs by applying the output carry of one stage to the next subsequent stage. The number of bits that are to be ripple carry added verdicts the number of gates and hence the other performance parameters. The figure 8 shows 4 Bit RCA

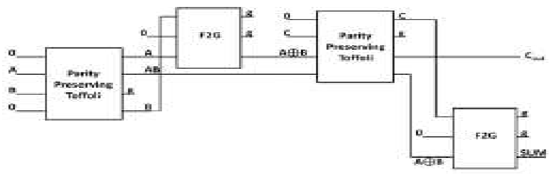

FIGURE 4: FAULT TOLERANT FULL ADDER USING PARITY PRESERVING TOFFOLI [16]

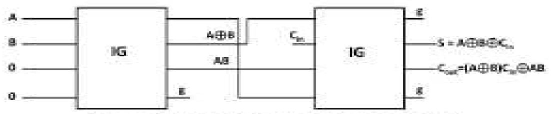

FIGURE 5: FAULT TOLERANT FULL ADDER IN [18]

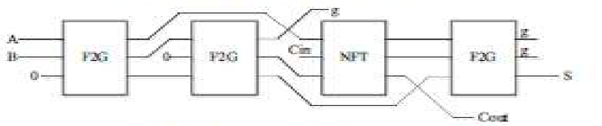

FIGURE 6: FAULT TOLERANT FULL ADDER IN [19]

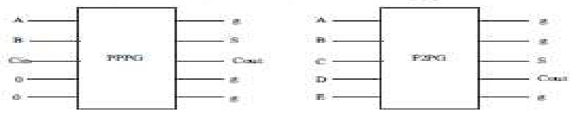

FIGURE 7: FAULT TOLERANT FULL ADDER IN [7] AND [13]

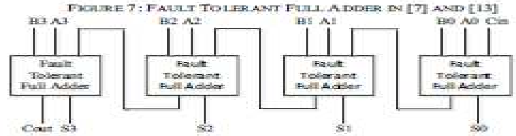

FIGURE 8: FAULT TOLERANT RIPPLE CARRY ADDER

Figure 4: Fault Tolerant Full Adder Using Parity Preserving, figure 5: Fault Tolerant Full Adder In [18], Figure 6: Fault Tolerant Full Adder In [19]
Figure 7: Fault Tolerant Full Adder In [7] And [13] Toffoli [16], Figure 8: Fault Tolerant Ripple Carry Adder

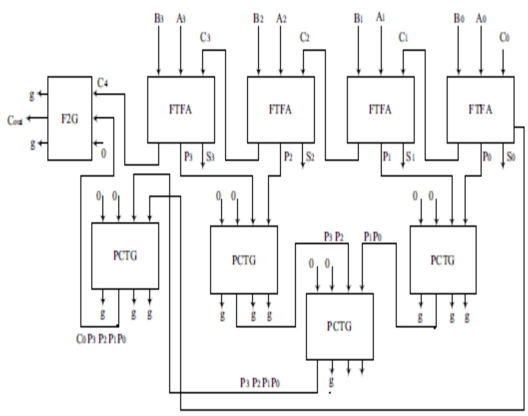

FIGURE 9: PROPOSED FOUR BIT PARITY PRESERVING CARRY SKIP ADDER DESIGN

Figure 9: Proposed Four Bit Parity Preserving Carry Skip Adder Design

The four bit carry skip adder design consists of 4 FTFAs which are used to produce carry propagates and sum bits and PCTGs which are used to compute the product of the carry propagates along with the Input carry. A carry skip adder reduces the carry propagation time by skipping over consecutive adder stages. The first FTFA inherently produces the fan-out for C0 required at the last stage of the circuitry.

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IV. PERFORMANCE ANALYSIS OF PROPOSED FAULT TOLERANT FULL ADDER AND RIPPLE CARRY ADDERS

A. Performance of Proposed Toffoli Structure

The Parity Conserving Toffoli Proposed has been studied and compared with the other such structures in the literature. The gate is unique in terms of its structure where it is a single gate that is used to construct the Toffoli as against other design which use a cascade of other conservative gates to design a conservative Toffoli. This inimitable
character optimizes all the parameters of the design namely the GC, CI, GO, QC, TRLIC
and Total Logic Cost T. The same are tabulated and the percentage improvements are calculated in Table 2. From the comparison it can be noticed that the proposed structure in [20] is the most optimized design.

Table 1: Comparison Of Toffoli Strucstructures And Percentage Improvements

TABLE 1: COMPARISON OF TOFFOLI STRUCTURES AND PERCENTAGE IMPROVEMENTS

Toffoli Structure → ↓Parameters	Proposed Design	Design in [18]	Design in [12]	Design in [17]
GC	1	2 (50%)	2 (50%)	3 (67%)
CI	1	1 (-)	1 (-)	2 (50%)
GO	1	1 (-)	1 (-)	2 (50%)
QC	7	7 (-)	7 (-)	9 (22%)
TRLIC	10	11(9%)	11(9%)	16 (38%)
T	$2\alpha+2\beta$	$4\alpha+4\beta+\delta$	$5\alpha+3\beta+2\delta$	$6\alpha+4\beta+2\delta$

B. Performance Evaluation of Adder Structures

The performance of the different adders can be premeditated by considering the logic cost of the reversible circuit. The fault tolerant full adder structure is obtained by substituting the Parity Conserving Toffoli in the generalized structure proposed in [16]. This fault tolerant full adder is subsequently used to design a ripple carry adder as in [20] and further used to propose 4 bit fault tolerant Carry Skip Adder.

The Total Logic Cost of the FTFA is $T = 8\alpha + 4\beta$, as it comprises of two PCTGs and two F2Gs. The different FTFAs in the literature have logic costs $12\alpha+8\beta+2\delta$ in [18], $14\alpha+6\beta+4\delta$ in [12], $16\alpha+8\beta+4\delta$ in [17], $8\alpha+6\beta+2\delta$ in [14], $8\alpha+16\beta+4\delta$ in [15], $9\alpha+4\beta+3\delta$ in [19], $11\alpha+18\beta+11\delta$ and $8\alpha+6\beta+2\delta$ in [7] and [13] respectively. The same are tabulated in Table 2. Thus the proposed design has the least logical cost than all those studied in the literature. Consequently it can be said that the design is the most optimized one. The ripple carry adder being the cascade of FTFAs is also optimized design. The 4 bit CSA design proposed consists of FTFA and the PCTGs along with F2G. The Total Logical cost of the CSA is $T= 42\alpha + 24\beta$, with fan-out being taken into consideration. The Cost metrics of the 4 bit CSA $T= 40\alpha + 28\beta+12\delta$ in [21] without taking fan-out into consideration. Had the design taken fan-out into account, the cost may further increase. $T=40\alpha+80\beta+20\delta$ in [15] after taking Fan-out into consideration. Thus the proposed design is again an optimized one in terms of the Total Logic Cost. The design proposed in [22] uses TSG and Fredkin gates to design the CSA, generating a total logic cost of $T=32\alpha+36\beta+44\delta$, Fan-out not being taken
into consideration. The comparison between the designs is shown in table 3.

The different structures are functionally tested for their logical correctness using XILINX in conjunction with MODELSIM and the simulation results are as shown in figures 10, 11, 12 and 13.

TABLE 2: COMPARISON OF FULL ADDER DESIGNS

Fault Tolerant Full Adder Design	Gates	Total Logical Cost
Proposed Design	2 PCTG+ 2 F2G	$T = 8\alpha + 4\beta$
Design in [14]	2 IG	$T = 8\alpha+6\beta+2\delta$
Design in [13]	1 F2PG	$T = 8\alpha+6\beta+2\delta$
Design in [15]	4 FRG	$T = 8\alpha+16\beta+4\delta$
Design in [19]	1 NFT +3 F2G	$T = 9\alpha+4\beta+3\delta$
Design in [18]	2 FRG +4 F2G	$T = 12\alpha+8\beta+2\delta$
Design in [12]	2 NFT +4 F2G	$T = 14\alpha+6\beta+4\delta$
Design in [17]	2 FRG+ 6 F2G	$T = 16\alpha+8\beta+4\delta$
Design in [7]	1 PPPG	$T = 11\alpha+18\beta+11\delta$

TABLE 3: COMPARISON OF 4 BIT RIPPLE CARRY ADDER DESIGNS

4 Bit Ripple Carry Adder Design	Gates	Total Logical Cost
Proposed Design	8 PCTG+ 8 F2G	$T = 32\alpha + 16\beta$
Design in [14]	8 IG	$T = 32\alpha +24\beta +8\delta$
Design in [13]	4 F2PG	$T = 32\alpha +24\beta +8\delta$
Design in [15]	16 FRG	$T = 32\alpha +64\beta +16\delta$
Design in [19]	4 NFT +12 F2G	$T = 36\alpha +16\beta+12\delta$
Design in [18]	8 FRG +16 F2G	$T = 48\alpha+32\beta+8\delta$
Design in [12]	8 NFT +16 F2G	$T = 56\alpha+24\beta+16\delta$
Design in [17]	8 FRG+ 24 F2G	$T = 64\alpha+32\beta+16\delta$
Design in [7]	4 PPPG	$T = 44\alpha+72\beta+44\delta$

TABLE 4: COMPARISON OF CSA DESIGNS

4 Bit Carry Skip Adder Design	Total Logical Cost	Conservative Nature	Fan-out
Proposed Design	$T = 42\alpha + 24\beta$	Yes	Yes
Design in [21]	$T = 40\alpha +28\beta +12\delta$	Yes	No
Design in [15]	$T = 40\alpha +80\beta +20\delta$	Yes	Yes
Design in [22]	$T = 32\alpha +36\beta +44\delta$	No	No

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V. CONCLUSION

In this paper the different adder structures namely full adder, ripple carry adder have been studied and the Carry skip adder have been designed, starting from the most elementary structure PCTG. This gate is the parity conservative cohort of the Toffoli gate. It maintains the universality of the Toffoli gate as well as inherits the conservative nature.

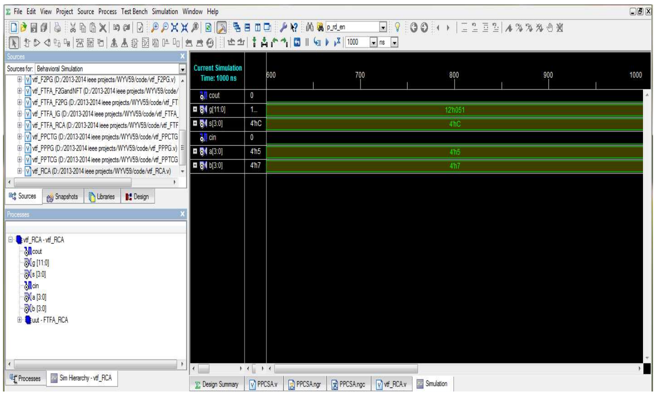

Figure 10: Simulation Results Of Proposed Parity Preserving Toffoli Structure

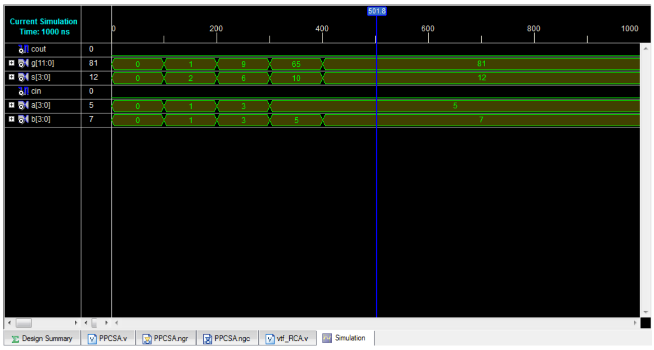

Figure 11: Simulation Results Of Proposed Parity Preserving Full Adder

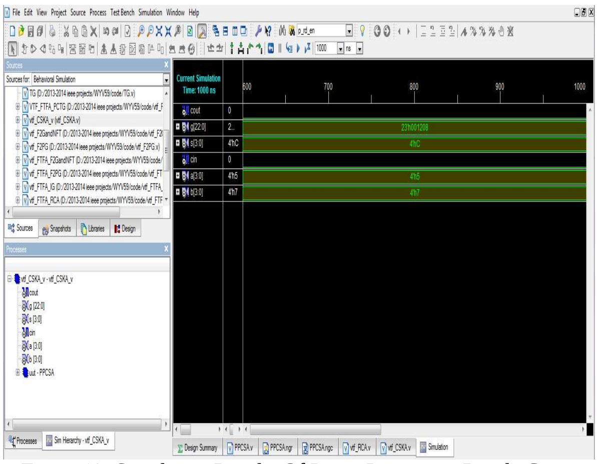

Figure 12: Simulation Results Of Parity Preserving Ripple Carry Adder

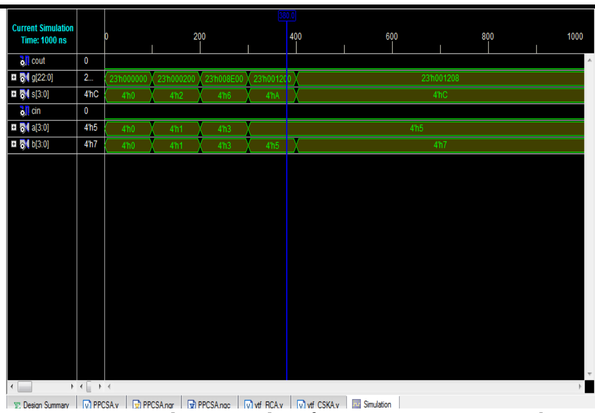

Figure 12: Simulation Results Of Parity Preserving Carry Skip Adder

The implementation of full adder, which is the most fundamental block of the high speed adders and the ALU, plays a key role in the design aspects of any complex system. In this view the complexity of the full adder itself needs to be minimized so that the complexity of the system reduces. It has been observed that the complexity can be measured using different yardsticks namely the gate count, the quantum cost and the TRLIC. Meanwhile these parameters' scale must be suitably supported by the hardware complexity of the design which is given by the Total Logic Cost. The proposed designs can be said to be the optimized one as they have been derived from the least logical cost PCTG. These structures may be implemented in quantum dot cellular automata, in order to pave a path for further research.

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REFERENCES

[1]. R. Landauer,"Irreversibility and Heat Generation in the Computational Process", IBM Journal of R&D,1961.
[2]. C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
[3]. A. Peres, Reversible logic and quantum computers, Phys. Rev. A 32 (1985) 3266–3276.
[4]. E. Fredkin and T. Toffoli,"Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982.
[5]. R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.
[6]. B. Parhami, "Fault tolerant reversible circuits", Asimolar Conf. Signal systems and computers", October 2006
[7]. Krishna Murthy, Gayatri G, Manoj Kumar "Design of Efficient Adder Circuits Using Proposed Parity Preserving Gate" VLSICS Vol.3, No.3, June 2012.
[8]. Md. Saiful Islam et.al" Synthesis of fault tolerant Reversible logic"IEEE 2009
[9]. Rakshith Saligram, Rakshith T R,"Novel code converters employing reversible logic", International Journal of Computer Applications, Vol. 52 Aug 2012.
[10]. Rakshith Saligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" International Journal of VLSI

International Journal of Advanced Research Foundation
Website: www.ijarf.com, Volume 2, Issue 8, August 2015)

Design and Communication systems, Dec-12
[11]. Rakshith T R and Rakshith Saligram, Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach, Intl. Conf. on Circuit, Power and Computational Technologies. March 2013.
[12]. Haghparast, M. and K. Navi, " A novel fault tolerant reversible gate for nanotechnology based systems". Am. J. Appl. Sci., 5(5).2008
[13]. Xuemei Qi and Et. Al, Design of fast fault tolerant reversible signed multiplier, International Journal of the Physical Sciences Vol. 7(17), pp.2506 - 2514, 23 April, 2012.
[14]. Md. Saiful Islam and Zerina Begum, "Reversible Logic Synthesis of Fault Tolerant Carry Skip BCD Adder"
[15]. J. W. BRUCE, M. A. THORNTON, L. SHIVAKUMARAIAH, P.S. KOKATE, X. LI, Efficient Adder Circuits Based on a Conservative Reversible Logic Gates, In Proc. of IEEE Computer Society Annual Symposium on VLSI, Pittsburg, PA, pp. 83-88, 2002.
[16]. M. Haghparast and K. Navi," Design of a Novel Fault Tolerant Reversible Full Adder for Nanotechnology Based Systems", World App.Sci. J., 3(1), pp. 114-118, 2008.
[17]. Parhami, B., 2006. Fault tolerant reversible circuits, Proc. 40th Asilomar Conf. Signals, Systems and Computers, October 2006, Pacific Grove, CA, pp: 1726-1729.
[18]. Md, Saiful Islam et.al, "Synthesis of Fault Tolerant Rveresible Logic Circuits", IEEE 2009.
[19]. Sajib Kumar Mitra, Ahsan Raja Chowdury, " Minimum Cost Fault Tolerant Full Adder Circuit in reversible logic synthesis", 25th Intl. Conf.on VLSI Design 2012.
[20]. Rakshith Saligram and Rakshith T.R." Deisgn of Low Logical Cost Adders using Novel Parity Conserving Toffoli Gate" 2013 IEEE Intl. Conf on Emerging trends on Communication, Control, Signal Processing and Computing Applications.
[21]. Md. Saiful Islam, Muhammad Mahbubur Rahman, Zerina begum, and Mohd. Zulfiquar HafizFault,"Tolerant Reversible Logic Synthesis : Carry Look-Ahead and Carry-Skip Adders", IEEE 2009.
[22]. Himanshu Thapliyal and M.B. Sreenivas, "A New Reversible TSG Gate and Its Application For Designing Efficient Adder Circuits".