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Energy Efficient Code Converters Using Reversible Logic Gates

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***Abstract:* - In this technological world development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In digital systems code conversion is a widely used process for reasons such as enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required, dropping the level of switching activity leading to more speed of operation and power saving etc. This paper proposes novel Reversible logic design for code conversion such as Binary to Gray code, Gray to Binary code, BCD to Excess 3 code, Excess 3 to BCD code.**

Keywords: - Reversible logic, efficient code converters, low power logic gates & VLSI design.

1. INTRODUCTION

Reversible computing is a model of computing where the computational process to some extent is reversible, i.e., time-invertible. A necessary condition for reversibility of a computational model is that the relation of the mapping states of transition functions to their successors should at all times be one-to-one. Reversible computing is generally considered an unconventional form of computing.

There are two major, closely related, types of reversibility that are of particular interest for this purpose: physical reversibility and logical reversibility.

A process is said to be physically reversible if it results in no increase in physical entropy; it is isentropic. These circuits are also referred to as charge recovery logic or adiabatic computing. Although in practice no stationary physical process can be exactly physically reversible or isentropic, there is no known limit to the closeness with which we can approach perfect reversibility, in systems that are sufficiently well-isolated from interactions with unknown external environments, when the laws of physics describing the system's evolution are precisely known.

Probably the largest motivation for the study of technologies aimed at actually implementing reversible computing is that they offer what is predicted to be the only potential way to improve the energy efficiency of computers beyond the fundamental von Neumann-Landauerlimit of kTln energy dissipated per irreversible bit operation.

As was first argued by Rolf Landauer of IBM, in order for a computational process to be physically reversible, it must also be logically reversible. Landauer's principle is the loosely formulated notion that the erasure of n bits of information must always incur a cost of nkln in thermodynamic entropy. A discrete, deterministic computational process is said to be logically reversible if the transition function that maps old computational states to new ones is a one-to-one function; i.e. the output logical states uniquely defines the input logical states of the computational operation.

For computational processes that are nondeterministic (in the sense of being probabilistic or random), the relation between old and new states is not a single-valued function, and the requirement needed to obtain physical reversibility becomes a slightly weaker condition, namely that the size of a given ensemble of possible initial computational states does not decrease, on average, as the computation proceeds forwards.

The reversibility of physics and reversible computing Landauer's principle (and indeed, the second law of thermodynamics itself) can also be understood to be a direct logical consequence of the underlying reversibility of physics, as is reflected in the general Hamiltonian formulation of mechanics, and in the unitary time-evolution operator of quantum mechanics more specifically.

In the context of reversible physics, the phenomenon of entropy increase (and the observed arrow of time) can be understood to be consequences of the fact that our evolved predictive capabilities are rather limited, and cannot keep perfect track of the exact reversible evolution of complex physical systems, especially since these systems are never perfectly isolated from an unknown external environment, and even the laws of physics themselves are still not known with complete precision. Thus, we (and physical observers generally) always accumulate some uncertainty about the state of physical systems, even if the system's true underlying dynamics is a perfectly reversible one that is subject to no entropy increase if viewed from a hypothetical omniscient perspective in which the dynamical laws are precisely known. The implementation of reversible computing thus amounts to learning how to characterize and control the physical dynamics of mechanisms to carry out desired computational operations so precisely that we can accumulate a negligible total amount of uncertainty regarding the complete physical

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state of the mechanism, per each logic operation that is performed. In other words, we would need to precisely track the state of the active energy that is involved in carrying out computational operations within the machine, and design the machine in such a way that the majority of this energy is recovered in an organized form that can be reused for subsequent operations, rather than being permitted to dissipate into the form of heat.

Although achieving this goal presents a significant challenge for the design, manufacturing, and characterization of ultra-precise new physical mechanisms for computing, there is at present no fundamental reason to think that this goal cannot eventually be accomplished, allowing us to someday build computers that generate much less than 1 bit's worth of physical entropy (and dissipate much less than kTln 2 energy to heat) for each useful logical operation that they carry out internally.

The motivation behind much of the research that has been done in reversible computing was the first seminal paper on the topic, which was published by Charles H. Bennett of IBM research in 1973. Today, the field has a substantial body of academic literature behind it. A wide variety of reversible device concepts, logic gates, electronic circuits, processor architectures, programming languages, and application algorithms have been designed and analyzed by physicists, electrical engineers, and computer scientists.

This field of research awaits the detailed development of a high-quality, cost-effective, nearly reversible logic device technology, one that includes highly energy-efficient clocking and synchronization mechanisms. This sort of solid engineering progress will be needed before the large body of theoretical research on reversible computing can find practical application in enabling real computer technology to circumvent the various near-term barriers to its energy efficiency, including the von Neumann-Landauer bound. This may only be circumvented by the use of logically reversible computing, due to the Second Law of Thermodynamics.

2. PROPOSED REVERSIBLE CODE CONVERTERS

Designing of reversible logic circuit is challenging task, since not enough number of gates are available for design. Reversible processor design needs its building blocks should be reversible in this view the designing of reversible code converters became essential one. In the digital domain, data or information is represented by a combination of 0's and 1's. A code is basically the pattern of these 0's and 1's used to represent the data. Code converters are a class of combinational digital circuits that are used to convert one type of code in to another. Some of the most prominently used codes in digital systems are Natural Binary Sequence, Binary Coded Decimal, Excess-3 Code, Gray Code, ASCII Code etc. Like any combinational digital circuit, a code converter can be implemented by using a circuitry of AND, OR and NOT gates. Here this paper focuses more on conversion of code between binary to gray and BCD to excess-3.

Binary to Gray code converters used to reduce switching activity by achieving single bit transition between logical sequences.

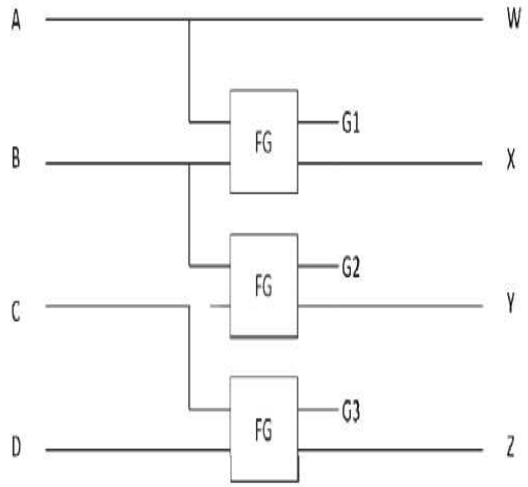

Figure 3.1 Circuit diagram of Reversible Binary to Gray code converter

If Input vector is I(D,C,B,A) then the output vector o(Z,Y,X,W). The circuit is constructed with the help of Feynman Gate (FG) gate[7], the Table 3.1 shows the truth table of FG gate and figure 3.1 & 3.2 shows the circuit diagram of reversible Binary to Gray code converter & Gray to Binary code converter.

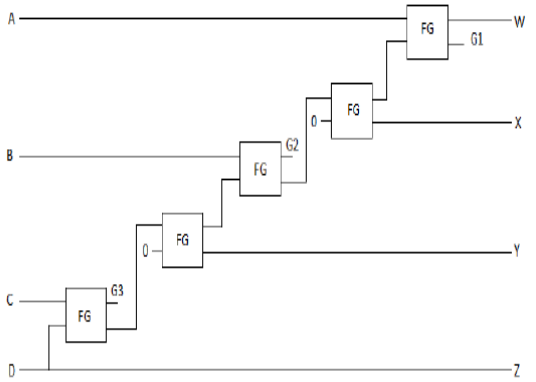

Figure 3.2 Circuit diagram of Reversible Gray to Binary converter

BCD to Excess-3 code converter used in arithmetic operational circuits to reduce the overall hardware complexity, The circuit is constructed with the help of two reversible gates Feynman Gate (FG) and Universal Reversible Gate (URG)[9]. The truth table of FG gate presented in session 3.1 and the truth table of URG gate presented in table 3.2 and the circuit diagram of Reversible BCD to Excess-3 and Excess-3 to BCD shown in figure 3.3 & 3.4 respectively.

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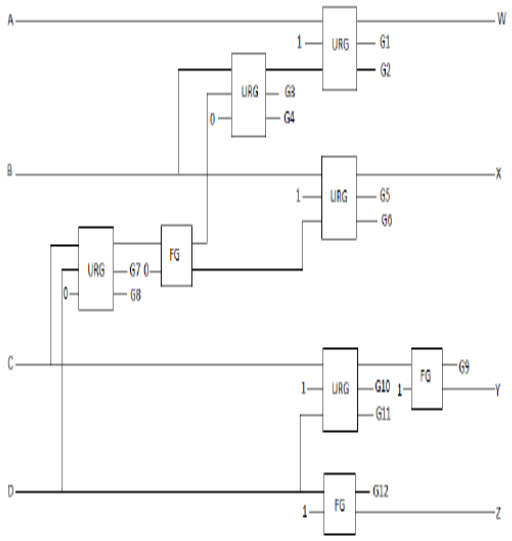


3.3 Circuit diagram of Reversible BCD to Excess-3 code converter

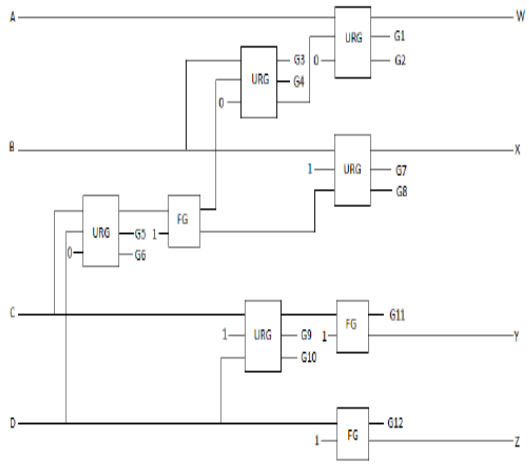


Figure 3.4 Circuit diagram of Reversible Excess-3 to BCD code converter

The proposed reversible code converter is more efficient then the conventional code converters. Evaluation of the proposed circuit can be comprehended easily with the help of the Table 3.3. the total logical operation involved in the proposed reversible code converter circuit is calculated with the help of following logical assignments

a = XOR logic
b = buffer
c = NOT logic
d = OR logic
e = AND logic

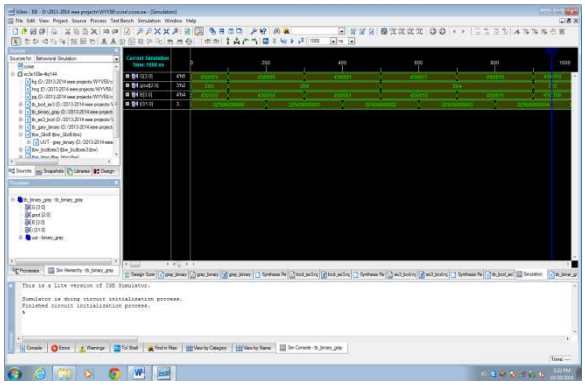
for example if T = 2a+3d then the circuit involves 2numbers of XOR logical operation and 3 numbers of OR logical operations. The performance of the design is based on the number of gate, number of garbage (not used terminals) and number of constants, in this proposed design the above said parameters are optimized to greater extent.

3. RESULT

Design Statistics

IOs : 20
Cell Usage:
BELS : 11
INV : 1
LUT2 : 5
LUT3 : 3
LUT4 : 1
VCC : 1
IO Buffers : 20
IBUF : 4
OBUF : 16

Device utilization summary:
Selected Device: 3s100etq144-4
Number of Slices: 5 out of 960 0%
Number of 4 input LUTs: 10 out of 1920 0%
Number of IOs: 20
Number of bonded IOBs: 20 out of 108 18%
Partition Resource Summary:
Speed Grade: -4
Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 6.750ns



4. CONCLUSION

This paper has introduced and proposed reversible logic gates and reversible circuits for realizing different code converters like BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary using reversible logic gates. The proposed design leads to the reduction of power consumption compared with conventional logic circuits, the design proposed is implemented with FG and URG gates only in near future with the invent of new RLG the power consumption may reduced to little more greater extent, not only that there will be a chance of implementing different logic circuits using reversible logic gates and which intern helps to increase the energy efficiency to a greater extent.

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