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Mach-Zehnder Interferometer based All Optical Reversible Carry-Look ahead Adder

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Abstract: **-In this work, we present an efficient reversible implementation of Carry-Lookahead Adder (CLA) in all-optical domain. Now-a-days, semiconductor optical amplifier (SOA)-based Mach–Zehnder interferometer (MZI) plays a vital role in the field of ultra-fast all-optical signal processing. We have used all optical based Mach-Zehnder Interferometer (MZI) switches to design the CLA circuit implementing reversible functionality. Two approaches are proposed for designing the CLA circuit. First, we propose a hierarchical approach for implementation of 2n-bit reversible CLA. In the second approach, we remove the drawback of hierarchical CLA and improve the design by implementing non-modular staircase structure of n-bit reversible CLA. The design complexities of both the approaches are computed. Experimental result shows that the optical cost and delay incurred in staircase structured reversible implementation of CLA are much less than those proposed in the recently reported works.**

Keywords: - Reversible computing, Mach-Zehnder Interferometer (MZI), Carry-lookahead Adder (CLA), optical cost, optical delay.

1. INTRODUCTION

Advances in VLSI technology and the use of new fabrication processes over the last few decades have rendered the heat dissipation problem more complex in deep-submicron integrated circuits (IC). If IC technology continues to follow the pattern predicted by the Moore's Law [15], the energy loss in non-reversible design is likely to become more dominant, and reversible logic may offer a viable solution in the future nanoscale technologies. According to Landauer's principle [16-17], a certain amount of energy (*KT* Joules/bit) is dissipated in traditional logic computation as heat due to the loss of every bit of information during the computing process. To encounter these problems, some alternate technologies are needed to design information lossless circuits. Bennet postulated [18-19] that the zero energy dissipation is only possible if the computation process is reversible under ideal condition. The inherent energy loss resulting from the irreversibility of information processing may be mitigated by implementing reversibility [14], which is information lossless. Hence, the reversible logic design has evolved as a potential solution with newer technologies replacing conventional logic design techniques.

In the present arena of computing technology, the optical computing has drawn the attention of the researchers over the last few years. Researchers are aiming at the development of optical digital computing system for processing binary data. Photons are the source of optical technology. This photonic particle provides unmatched speed with information as it has the speed of light. The optical components in the electronic computer system produce optical electronic hybrid network. The design of reversible circuit with optical technology can be implemented using Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switch, which has significant advantages of high speed, low power, fast switching time and ease of fabrication.

The optical implementation of MZI based reversible logic gates such as Toffoli [3], Feynman [12], and Fredkin [13] have already been reported in [6-7]. The design of Fredkin has been presented based on TOAD (terahertz optical asymmetric demultiplexer) in [8] and all-optical fiber in [11]. Design of single ancillary qubit based linear-depth quantum adder circuit that performs ripple-carry addition is presented in [2]. The reversible garbage free arithmetic logic unit implementing combined quantum arithmetic and logical operation in a single unit is presented in [1]. An optimized architecture of reversible BCD adder is demonstrated in [4]. In this design, minimum number of ancilla inputs and garbage output lines has been used to design the adder. Optical implementation of functionally reversible Mach-Zehnder Interferometer based Binary Adder has been proposed in [5], where two new optical reversible gate ORG-I and ORG-II have been proposed in addition to existing Feynman gate to design the architecture. All-optical XOR gate using SOA-based MZI and micro resonators has been implemented in [9] and [10], respectively. In this work, we propose an efficient reversible [20] implementation of Carry-Look ahead Adder (CLA) using optical technology. The proposed implementation has two merits. First, proposed design does not need any ancilla (extra lines) lines. Secondly, this design provides drastic reduction in optical cost and delay compared to the earlier designs.

The rest of the work is organized as follows. Section 2 presents brief reviews on the fundamental of reversible logic and reversible optical circuits. Proposed technique and

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complexity analysis are discussed in section 3. Finally, section 4 concludes the discussion.

2. BACKGROUND

A. Reversibility:

A fan-out free circuit (*Cnf*) with circuit depth (d) over the setof input lines *X, where X={x1, x2, …,xn}* is said to be reversible(Rc) if the mapping from input to output is bijective (*f : Bm_Bn*) and the number of inputs (*m*) is equal to number of outputs (*n*) i.e *m = n* and also the circuit consists of reversible gates (*gi*) only i.e. *Cnf = g0 .g1.g2 . … .g(d-1)*, where *gi* represents *ith* reversible gate of the circuit.

B. MZI Architecture:

Design of reversible logic gates like NOT, *k*-CNOT, Toffoli, Fredkin, Peres gates is possible in many ways. Among them, the quantum and optical technology are two very prominent implementation mediums. From the quantum technology point of view, the basic quantum gates such as NOT, CNOT, V and V+ are used to design reversible gates. In optical technology, MZI based optical switches are used to implement reversible gates. An optical MZI switch can be designed [9] using two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (*C-1, C-2*) as shown in Fig. 1. MZI switch has two inputs ports namely, A and B and two output ports called as bar port and cross port, respectively. The optical signals coming at port B and port A at the input side are control signal (_2), and incoming signal (_1), respectively. The working principle of a MZI is explained as follows:

When there is a presence of incoming signal at port A and control signal at port B, then a light would appear at the output bar port and no light would appear at the output cross port. Again on absence of control signal at input port B and presence of incoming signal at input port A, the light would appear at the output cross port and no light would appear at the output bar port.

The logic value of the absence of light and presence of light is denoted by 0 and 1, respectively. From the point of view of boolean function, the above behaviour of MZI switch can be written as P (Bar Port) =*A.B* and Q (Cross Port) =*A*Bbar

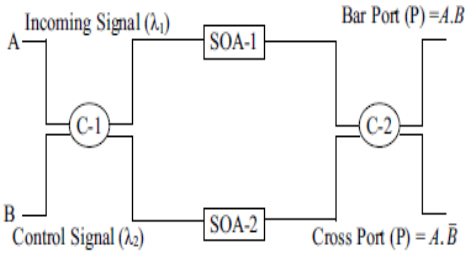

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Fig. 1: Semiconductor Optical Amplifier based MZI Switch

C. Beam Combiner (BC) and Beam Splitter (BS):

Beam combiner (BC) simply combines the optical beams while the beam splitter (BS) splits the beams into two optical beams. The optical cost and the delay of beam combiner and beam splitter are negligible [4, 6] and while calculating optical cost of a circuit, it may be assumed as zero.

In the schematic diagram of various circuits in section 3, the beam combiner (BC) and beam splitter (BS) are represented by hollow bubble (o) and solid bubble (•) respectively.

D. Optical cost and delay

As the optical cost of BS and BC are relatively small, the optical cost of a given circuit is the number of MZI switches required to design the realization. The optical delay is estimated as the number of stages of MZI switches multiplied by a unit Δ.

The Feynman gate (FG) is a 2 inputs and 2 outputs reversible gate where the light from input A is incident on beam splitter (BS) and is split into two parts as shown in Fig. 2(a). One part enters into MZI-1 and acts as control signal; whereas other light beam is incident on MZI-2 and acts as incoming signal. In the similar way, the light signal from input B is connected to MZI-1 and MZI-2 as shown in Fig. 2(a). The light from bar port of MZI-1 (B1), MZI-2 (B2) and a part of light from the cross port of MZI-2 (C2) are combined by BC-1 to get the final output P. The light from cross port of MZI-1 (C1) andMZI-2 (C2) are combined by BC-2 to get the final output Q that complements the value appeared at port B only when the input signal A=1.

MZI-based optical design of reversible Toffoli gate is depicted in Fig. 2(b). Standard optical costs and delay ratings [6] of few reversible gate benchmarks are presented in Table-I.

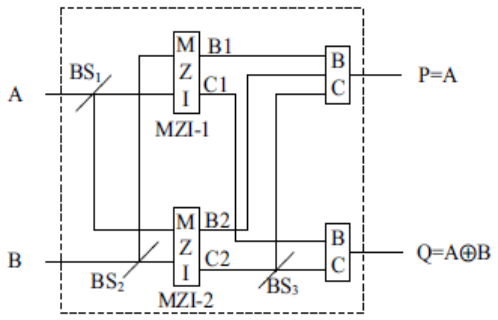

Fig. 2(a): MZI based optical implementation of Feynman gate

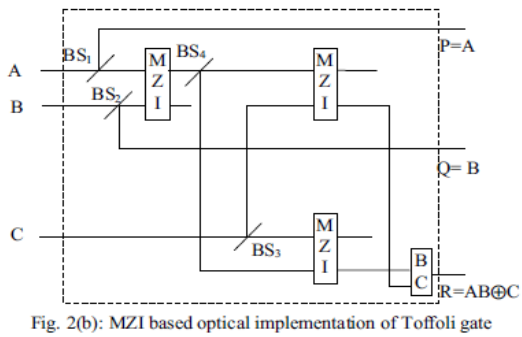

Fig. 2(b): MZI based optical implementation of Toffoli gate

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Table-I: Optical cost and delay of reversible gates [6]

	No. of MZI	No. of BS	No. of BC	Optical Cost	Delay
Feynman gate	2	3	2	2	Δ
Toffoli gate	3	4	1	3	2Δ
Fredkin gate	2	1	2	2	Δ
Peres gate	4	5	3	4	2Δ

3. PROPOSED TECHNIQUE

In this section, we present all optical reversible implementation of Carry Lookahead Adder (CLA) with the property of functional reversibility using Mach-Zehnder Interferometer (MZI) switches. We have proposed two design techniques of CLA: - one is hierarchical implementation and another is non modular staircase structured implementation. In hierarchical implementation, a generalised design of all optical reversible CLA using SOA-based MZI switches is presented. The design of reversible CLA is improved by introducing staircase structure. These techniques are discussed in details.

A. Hierarchical design of 2^n -bit CLA

This design is divided in two phases. In initial phase, we design an optimized 4-bit CLA circuit and consider this 4-bit design as basic building block. Integrating several small 4-bit CLA blocks in a hierarchical way, a 2^n-bit CLA circuit is constructed.

A.1. Optimized 4-bit CLA Design with MZI

A reversible full adder circuit implemented with 4 MZI switches, 4 *beam splitters (BS)* and 3 *beam combiners (BC)* as shown in Fig. 3(a). Here, apart from sum (*Si*) and carry (*Ci*), we define two extra variables: - *carry generator* (*Gi*) and *carry propagator* (*Pi*), where $Gi = ai.bi$ and $Pi = ai \oplus bi$. The carry generate (*Gi*) generates output carry when the bit values of both the input namely, *ai* and *bi* are set to one, where the carry propagate *(Pi)* helps to propagate the carry from *Ci* to *Ci+1*. The output sum (*Si*) and carry (*Ci*) are expressed as $Si = Pi \oplus Ci$ and $Ci+1 = Gi + PiCi$.

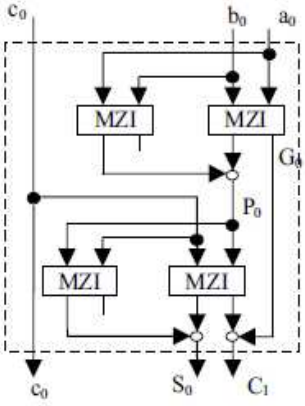

Fig. 3(a): Full adder circuit

The optimized design of 4-bit CLA circuit using MZI switches is shown in Fig. 3(b). This circuit consists of four full adder circuits as shown by the dotted box [Fig. 3(b)]. In CLA, there are two blocks: - one is *carry generate* block, and another is *carry propagate* block. The inputs to the 4 bit CLA are *A* (*a3a2a1a0*), *B* (*b3b2b1b0*) and *c0*. The *c0* acts as input carry. This 4-bit CLA performs addition of two four bit binary numbers. The outputs from the CLA are sum (*S*) and carry (*C*). We deduce the following relations from Fig. 3(b).

$$S_0 = P_0 \oplus C_0, \text{where } P_0 = a_0 \oplus b_0 \text{ and } C_0 = c_0$$
$$S_1 = P_1 \oplus C_1, \text{where } P_1 = a_1 \oplus b_1 \text{ and } C_1 = G_0 + P_0 C_0$$
$$S_2 = P_2 \oplus C_2, \text{where } P_2 = a_2 \oplus b_2 \text{ and } C_2 = G_1 + P_1 C_1$$
$$S_3 = P_3 \oplus C_3, \text{where } P_3 = a_3 \oplus b_3 \text{ and } C_3 = G_2 + P_2 C_2 .$$

A.2. 2^n-bit CLA Design

We integrate several 4-bit CLA in a hierarchical fashion to design a 2*n*-bit CLA circuit. In this hierarchical structure, we use two parameters namely, *group generate* and *group* 4-bit CLA modules and one additional 4-bit look-ahead block. The additional look-ahead block computes carry bits based on received *group generate* and *group propagate* values. Among the five 4-bit CLA modules, four CLA blocks are identical in the sense that they compute *group generate* and *group propagate* values but the fifth one does not. For a 4-bit CLA block, the group *generate* and *group propagate* functions are labelled as *G*0-3 and *P*0-3, respectively. The *group generate* and *group propagate* functions are defined as follows.

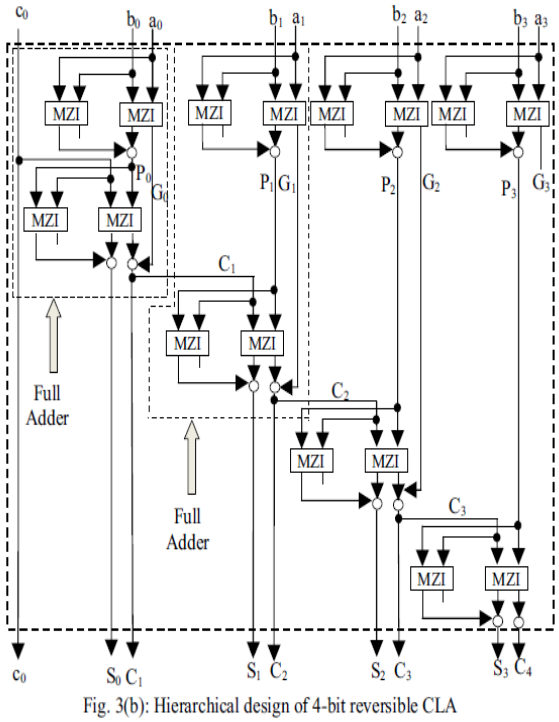

Fig. 3(b): Hierarchical design of 4-bit reversible CLA

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The *group generate* and *group propagate* functions are defined as follows.

$$G_{0,3}= G_3+G_2P_3+G_1P_2P_3+G_0P_1P_2P_3$$
$$P_{0,3} = P_0P_1P_2P_3.$$

In this way, we can construct higher order 2^n-bit CLA circuit using multiple 4-bit look-ahead blocks. For example, a 64-bit CLA is constructed by four 16-bit CLA and a 4-bit look-ahead block i.e. twenty-one 4-bit look-ahead block is required. Mathematically, we compute the expression for number of 4-bit look-ahead blocks required to design 2^n-bit CLA as follows.

Number of 4-bit CLA Blocks = (2^n/4 no. of 4-bit blocks) + (no. of 4-bit look-ahead blocks to design 2^{n-2}-bit CLA).

As the optical cost of a given circuit is the number of MZI switches required to design the realization, it is necessary to count the number of MZI switches in the given circuit for calculation of the optical cost of a CLA. Two separate situations can arise for calculation of optical cost of a 2^n-bit CLA.

Case 1*: Number of MZI switches to design 4-bit CLA* Total 16 MZI switches are required to design a 4-bit CLA as shown in Fig. 3(b). Hence, the optical cost of 4 bit CLA is 16.

Case 2: *Number of MZI switches to design 4^{i+1} -bit CLA* To design a 2^n-bit CLA circuit, where i >1 and $2^n = 4^{i+1}$, total number of MZI is computed as follows

Optical Cost=total number of MZI switches = (4 × (Number of MZI required for 4^i-bit CLA circuit) + 18*i* +3), where *n* represents number of bits and *i* is a positive integer indicating order index value.

Example 1: Calculate the total number of required MZI to implement 16-bit (2^n = 16) CLA circuit. First, we compute the order index value *i* as given below.

$$4^{i+1}=16, \text{ as } 2^n=4^{i+1}$$
$$\Rightarrow 4^{i+1}=4^2$$
$$\Rightarrow i+1=2$$
$$\Rightarrow i=1$$

Hence, the order index's value *i* for 16-bit CLA is 1. So, number of MZI required in 16-bit CLA circuit in hierarchical design =(4× (No. of MZI for 4^i-bit CLA circuit) + 18*i* +3)

$$= (4\times (\text{Number of MZI required to design } 4^1 \text{ -bit CLA circuit}) + 18\times 1 + 3)$$
$$= (4\times(\text{Number of MZI required to design 4 -bit CLA circuit}) + 21)$$
$$= ((4\times 16)+21) = 85$$

We have already calculated the required number of MZI to design *m*-bit hierarchical CLA circuit, where *m* is the order of 4. But when we are designing an *m*-bit CLA circuit, where

$$m \in \{\{2^j\}-\{4^{\lceil j/2 \rceil}\}\} \text{ or say } m \in 2^j \text{ but } m \notin 4^{\lceil j/2 \rceil} \text{ and } j \geq 2$$

(like *m*=8 or 32), then we will compute the required no. of MZI as well as optical cost for *m*-bit CLA circuit using the following formula. For a hierarchical design of 2×4^i-bit CLA circuit, the required no. of MZI = (2×(Number of MZI required designing a 4*i*-bit CLA circuit) + 6i +3).

Though we have seen two different expressions for calculating the optical cost (no. of MZI) of a 2*n*-bit CLA, but the optical delay is constant for the 2^n-bit CLA, that is (2^n +1) Δ But there are some limitations in this hierarchical design. When the number of bits to be added are large (2*n* > 64), then the design complexity increases due to the propagation of group generate and *group propagate* values in the circuit. To generate one *group generate* and one *group propagate* value,

we require additional 6 MZI switches as shown Fig. 3(c) marked by dotted box. In a 16-bit CLA circuit, we have required three *group generate* and three *group propagate* values. Hence to implement a 16-bit reversible CLA circuit in hierarchical manner, additional (3×6) or 18 MZI switches are required. Again, when we implement higher order (2^n bit, where $n\geq7$) CLA circuit, then the requirement of number of MZI switches is more. This problem is overcome by an improved design of CLA as described in next section.

B. Staircase Design of n-bit CLA

In the hierarchical design, the number of MZI switches increase due to the presence of *group generate* and *group propagate* functions. To overcome this, we propose an improved *n*-bit staircase structured CLA circuit that ensures use of minimum number of MZI along with optimized delay. In this approach, we remove the concept of *group generate* and *group propagate* function and present a staircase architecture for *n*-bit CLA circuit. We consider two *n*-bit binary numbers, *A*(*an-1an-2...a2a1a0*) and *B*(*bn-1bn-2...b2b1b0*) to be added using a *n*-bit staircase structured reversible CLA, where *Si* and *Ci* are the output sum and carry of *i*th input bits respectively. Then, *S0* = *P0*⊕ *C0*, where *P0* =*a0*⊕ *b0* as *C0*=*c0*=*0*. Hence, the modified *S0* is expressed as follows.

$$S_0= P_0\oplus 0= P_0$$
$$S_1 = P_1\oplus C_1, \text{where } P_1=a_1\oplus b_1 \text{ and } C_1 = G_0+ P_0C_0.$$
$$\text{As } C_0=c_0=0, \text{ the modified } C_1 \text{ is expressed as follows.}$$
$$C_1 = G_0+0 =G_0$$
$$S_2 = P_2\oplus C_2, \text{where } P_2=a_2\oplus b_2 \text{ and } C_2 = G_1+ P_1C_1$$
$$S_3 = P_3\oplus C_3, \text{where } P_3=a_3\oplus b_3 \text{ and } C_3 = G_2+ P_2C_2$$
$$\vdots$$
$$S_{n-2}=P_{n-2}\oplus C_{n-2}, \text{where } P_{n-2}=a_{n-2}\oplus b_{n-2} \text{ and } C_{n-2}=G_{n-3}+P_{n-3}C_{n-3}$$
$$S_{n-1}=P_{n-1}\oplus C_{n-1}, \text{where } P_{n-1}=a_{n-1}\oplus b_{n-1} \text{ and } C_{n-1}=G_{n-2}+P_{n-2}C_{n-2}$$

B.1. Optical Cost

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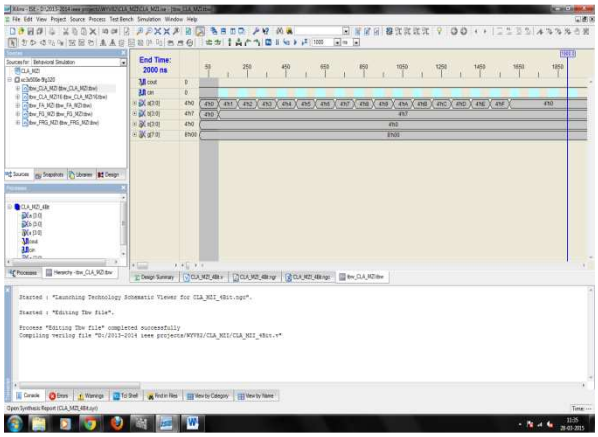
To add two single bit numbers using improved staircase CLA circuit, 2 MZI switches are required to generate *Gi* and *Pi* as shown in Fig. 4. Similarly, for addition of two *n*-bit numbers, *n* number of *Gi* and *Pi* is needed. Therefore to generate *n* number of *Gi* and *Pi*, total 2*n* number of MZI switches is required. Again, additional (*n*-1) carry bits are required to add two *n*-bit numbers and for each carry bit, 2 MZI switches are required. The required total number of MZI switches for (*n*-1) carry bits is {2×(*n*-1)}. Therefore, total [2*n* + {2×(*n*-1)}] or (4*n*-2) number of MZI switches is needed to implement an *n*bit CLA circuit. Hence, the optical cost of an improved *n*-bit CLA circuit is (4*n*-2).

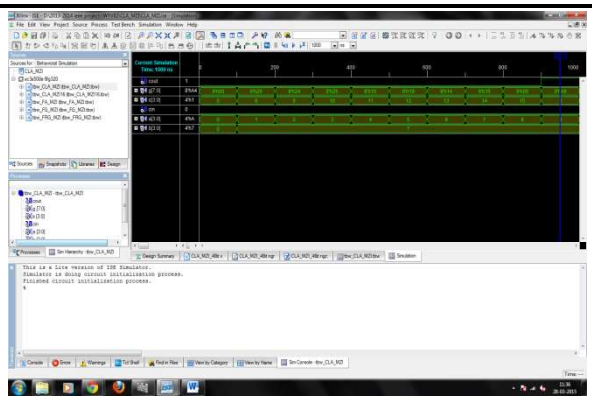
B.2. Calculation of Optical Delay

In an improved *n*-bit staircase structured reversible CLA circuit, *n* number of *Gi* , *Pi* and (*n*-1) number of carry bits (*C1*, *C2*, *C3* ….*Cn-1*) are generated, where *i*□€{0, 1, 2,…, *n*-1}. The values of *Gi* and *Pi* depend only on the values of input bits to be added, as *Gi = ai.bi* and *Pi =ai* ⊕ *bi*, where *ai* and *bi* are the input bits. As we get all the input bits at the same time, all the values of *Gi* and *Pi* are calculated concurrently i.e. if time required to calculate one *Gi* and *Pi* is Δ, then time required to calculate *n* numbers of *Gi* and *Pi* is also Δ.Again, the value of carry bit (*Ci+1*) depends on the value of the previous carry bit (*Ci*) value as *Ci+1 = Gi + CiPi*. Hence, all the values of *Ci* is sequentially calculated i.e. if time required to calculate one *Ci* is Δ, then time required to calculate *n* number of *Ci* is *n*×Δ . So, to generate (*n*-1) carry bit sequentially, the optical delay is (*n*-1)× Δ. Therefore, total optical delay to implement *n*-bit CLA circuit is {Δ+ (*n*-1) Δ} or *n*_ as shown in Fig. 4. A comparison of optical cost and delay of improved design of *n*-bit reversible CLA circuit with recently reported works is presented in Table-II. Experimental result shows that our design of improved CLA circuit is much more efficient than the adders presented in [1-2], [4-5]. This design is efficient not only in terms of optical cost but also in terms of optical delay.

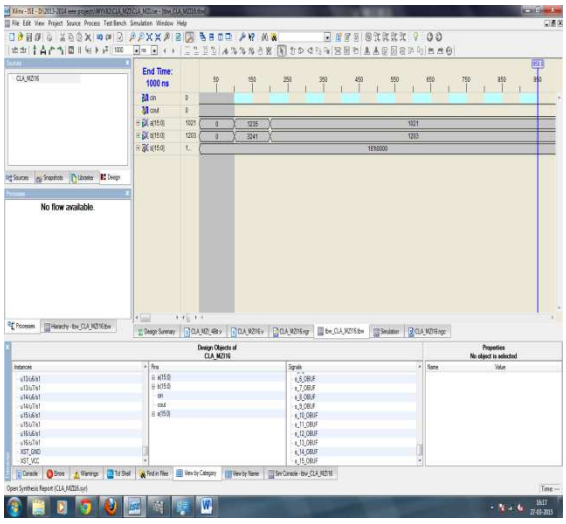
4. SIMULATION:

4 Bit TBW:

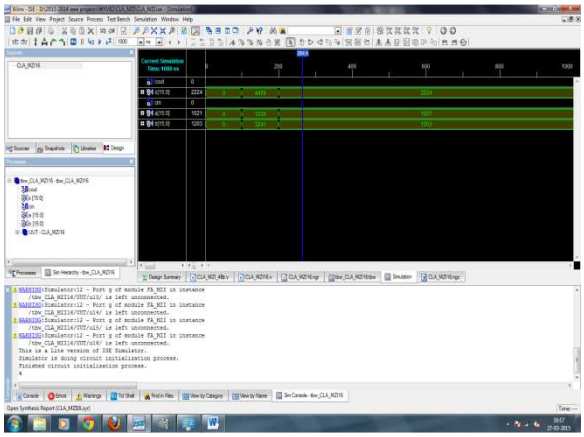




16 Bit TBW:



SIMULATED OUTPUT



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