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Design of High Speed 64-Bit MIPS Soft-Core Processor

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***Abstract*— This paper presents a run-time loading technique for a 64-bit MIPS (Microprocessor without Interlocked Pipeline Stages) processor. The update of MIPS code is done without having to resynthesize, place and route, and reload the soft-core. The design consists of three main blocks: a microprocessor soft-core, a software tool and a universal asynchronous receiver or transmitter (UART). The software tools set the content of the instruction memory space of the processor without having to go through the FPGA implementation process. The software tool communicates with the soft-core via UART. To demonstrate the proposed technique, assembly codes for several basic operations are performed. The design architecture is coded using Verilog based on top-down hierarchical design methodology using Xilinx ISE 13.2. The minimum delay is found to be 20.150ns and area is also minimized.**

***Index Terms*—MIPS, UART, RISC, Verilog, Xilinx ISE 13.2.**

I. INTRODUCTION

A processor is nothing but a logic or electronic circuitry that responds to and processes the basic instructions of a computer program by performing the arithmetic, logical, control and input or output (I/O) operations in order to drive a computer. The term central processing unit (CPU) is replaced by the term processor and sometimes is simply referred as the central processor. It is well thought-out as the brains of the computer where most of the calculations takes place and is the most important element of a computer system.

A microprocessor is an adaptable, multipurpose, programmable silicon chip that incorporates the functions of a CPU on single or few integrated circuits (IC). They are used in personal computers as well as many embedded systems because of its high speed. Added advantages of microprocessors are that it can speedily move data between the memory locations and also perform complex mathematical operations such as operating on floating point numbers. A microprocessor control program can be easily customized to different requirements of a product line, by enhancing the performance with minimum redesign of the product. With least production cost different features can be implemented in different models of a product line.

MIPS (originally an acronym for Microprocessor without Interlocked Pipeline Stages) developed by MIPS technologies. It is a reduced instruction set computer (RISC) instruction set architecture (ISA) that makes the processor design simpler by eliminating hardware interlocks between the pipeline stages. Earlier MIPS architectures were 32 bit, and later 64 bit versions were added. It is extensively used in digital cameras, wireless phones, HDTVs, DVD players, routers, etc. One of the most attractive applications of the MIPS architecture is its use in supercomputers.

A soft-core processor also called as soft microprocessor is implemented via different semiconductor devices containing programmable logic such as ASIC, FPGA, CPLD). It offers numerous advantages such as flexibility, platform independence, reduced cost, greater immunity to obsolescence. It can be tailored and tuned to specific needs, custom instructions more features, etc. The only disadvantage is the limited speed of the fabric.

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II. PROPOSED WORK

The microprocessor used is based on MIPS 64-bit architecture. The main blocks in the CPU are shown in Figure 2.1. The current microprocessor doesn't support Real-Time (RT) loading because the instruction memory is ROM module which means cannot be rewritable. The only way to updated the program is in the synthesis time. However, to make it supports RT loading; the instruction memory should be made rewritable in run time. Some logic has to be added in the instruction memory module to support RT L and the ROM logic has to be changed to RAM.

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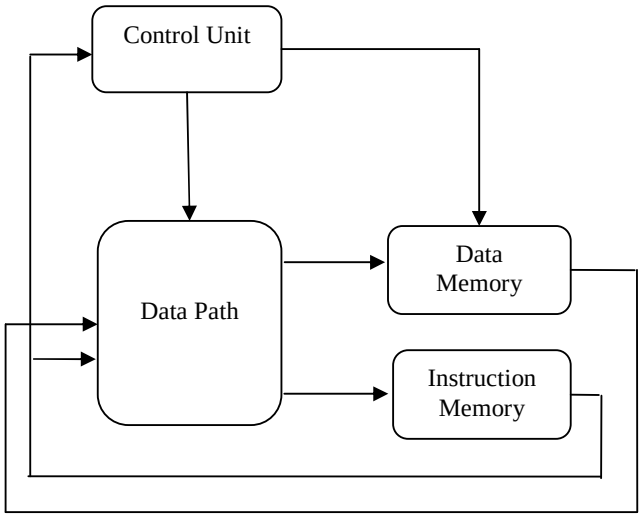

Figure 2.1 Proposed block diagram MIPS 64-Bit

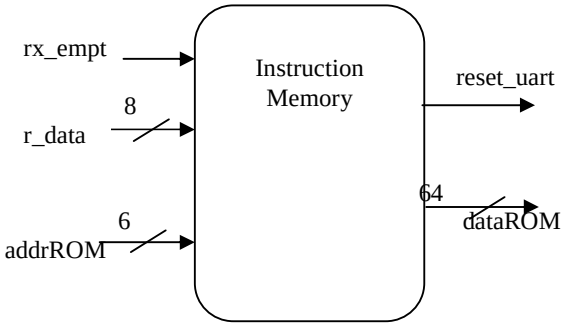

Figure 2.2 Block diagram of Instruction Memory

III. SIMULATION & SYNTHESIS RESULTS

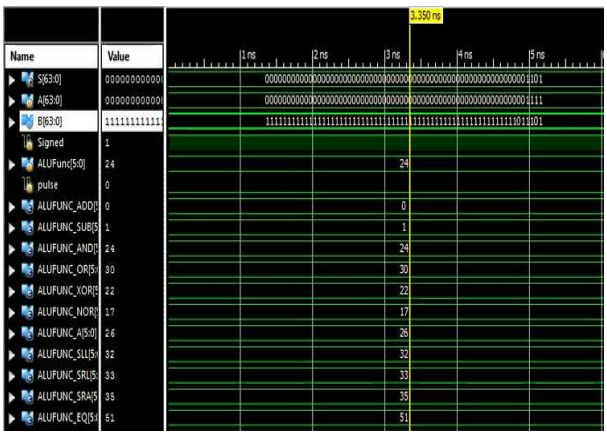

Figure 3.1 Simulation result of AND logic operation

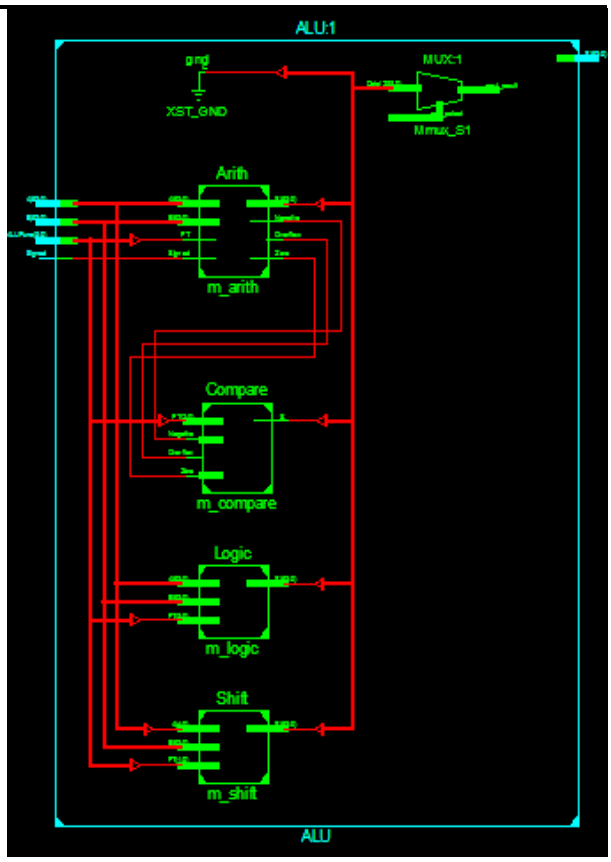

Figure 3.2 RTL schematic of 64-Bit ALU

HDL Synthesis Report

Macro Statistics
Adders/Subtractors : 3
64-bit adder : 3
Comparators : 3
64-bit comparator equal : 3
Multiplexers : 2
1-bit 8-to-1 multiplexer : 1
64-bit 4-to-1 multiplexer : 1
Xors : 4
1-bit xor2 : 3
64-bit xor2 : 1

Design Statistics
IOs : 199

Cell Usage :
BELS : 1313
GND : 1
INV : 1
LUT2 : 166
LUT3 : 186

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#	LUT4	: 490
#	MUXCY	: 158
#	MUXF5	: 181
#	MUXF6	: 1
#	VCC	: 1
#	XORCY	: 128
# IO Buffers		: 199
#	IBUF	: 135
#	OBUF	: 64

Device utilization summary:

Selected Device : 3s500efg320-4

Number of Slices:	465	out of	4656	9%
Number of 4 input LUTs:	843	out of	9312	9%
Number of IOs:	199			
Number of bonded IOBs:	199	out of	232	85%

Delay: **20.150ns (Levels of Logic = 76)**
Total 20.150ns (15.667ns logic, 4.483ns route)
(77.8% logic, 22.2% route)

Total memory usage is 200176 kilobytes

IV. CONCLUSION

In this paper the design architecture is coded for 64 bit MIPS soft-core processor using Verilog based on top-down hierarchical design methodology using Xilinx ISE 13.2. The minimum delay is found to be 20.150ns and area is also minimized.

REFERENCES

[1]. Mazen Bahaidarah et, al., "A novel technique for run time loading for MIPS soft core processor", 978-1-4673-6195-8/13/$31.00©2013IEEE.
[2]. Xizhi Li and Tiecai Li, "ECOMIPS: An Economic MIPS CPU Design on FPGA", Proceedings of the 4th IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC'04) 0-7695-2182-7/04 $ 20.00 IEEE.
[3]. Mrs. Rupali S. Balpande, "Design of FPGA based Instruction Fetch & Decode Module of 32-bit RISC (MIPS) Processor. 2011 International Conference on Communication Systems and Network Technologies. 978-0-7695-4437-3/11 $26.00 © 2011 IEEE.
[4]. Prathibha S R, M Z Kurian, "REALIZATION OF HIGH PERFORMANCE RUN-TIME LOADABLE MIPS SOFT-CORE PROCESSOR", IJRET: International Journal of Research in Engineering and Technology eISSN: 2319-1163 | pISSN: 2321-7308.
[5]. R.Nithya et, al., "Run-Time Reconfiguration of Processing Elements through Soft-Core Processor", International Conference on Communication and Signal Processing, April 3-5, 2014, India. 978-1-4799-3 3 5 8-7114/$3 1. 00 ©2014 IEEE.