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Design of A Multiband Flexible Divider Using A Low Power Single Phase Clock Distribution Network

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***Abstract*- The clock distribution network is the only signal which has the highest switching activity and it consumes 70% of total power consumed by an IC. The development of multiple PLL is to cater the need for a multiple clock domain network, the aim of the paper is to develop a low power single clock multiband network that supplies for multiple clock domains. The pulse swallow topology can be applied using WLAN frequency synthesizer and design can be modeled using verilog simulation that is implemented in FPGA . Bluetooth, zigbee etc. are some of the communication applications that are useful for this paper. By designing a Johnson counter and Ring counter we have proved that the counter designed with pulse enhancement scheme provides low power consumption in the counters.**

***Index Terms:* DFF, Extended TSPC (ETSPC), Frequency divider, counters, power delay product, prescaler**.

I. INTRODUCTION

One of the most important application of any flip flop is frequency division. Any frequency synthesizer is implemented by phase locked loop (PLL) and this uses prescaler. The prescaler need to work at low operating voltage as well as high frequency because the supply voltage and channel length reduces as process technology reduces. In frequency synthesizer the first stage divider is used as E-TSPC prescaler or some time dynamic latches are used as first stage for SLC divider. In frequency synthesizer, first stage frequency divider consumes more power, since it is implemented by a PLL[1]. flip flop consumes 30-50% also a power hungry block in RF front end. As the level of integration increases, the demand for low power, low cost multiband FR circuits also increases in this paper dynamic latches are used since it faster and consumes less power then static latches. The dynamic latch includes TSPC and E-TSPC designs that avoids skew problem. The high performance circuit power can be reduced by an effective method called clock distribution, the difficulty of clock tree optimization has been increased by development of gated cells[2]. The physical implementation of clock distribution network, controlling of clock skew, selection of sequential elements and decision on the topology are the different aspects of clock network design.

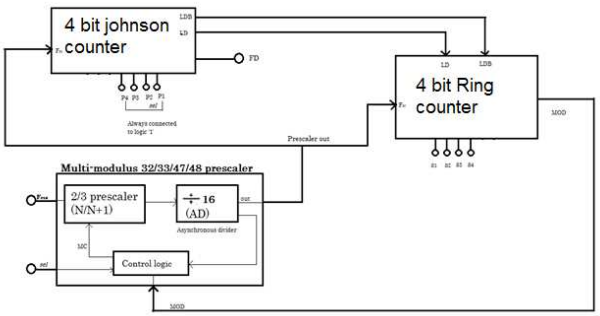

Fig1. General Block Diagram for the Proposed Technique

II.PREVIOUS WORK

With standard cells and high speed potentials it is easy to design a circuit with true single phase clock logic techniques that has alternative N and P logic cells. The sum of evaluation times is the critical path delay with a single logic block this is considered as advantage of asynchronous logic since there is no wastage of time for waiting, latches or other redundant logic. But the disadvantage is that it has high power consumption and difficult clock tree design. The dual rail or different styles are used to analyze every logic function this in turn increases clock load. hence we develop an extended method to speed up the dynamic single clock circuit. In order to minimize the unused time per clock cycle small asynchronous chains of dynamic logic blocks has been combined into one single period of global clock[3]. Hence this method has the advantage of power reduction by smaller clock trees and no need for latches, shorter latencies for calculation and a simpler clock distribution network. When compared with TSPC which has , the latency reduction is of 40% and power reduction for clock tree is 89% the simulation of E-TSPC has enhancement in power reduction of 40% for the logic. Along with clock here a multi-modulus prescaler is used for different applications in order to overcome the problem. Previous work had used the 7-bit programmable counter and 6-bit swallow counter, so to overcome the problem of delay, alternative counters has been implemented.

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III. PROPOSED WORK

Here in the present paper the Johnson counter and ring counter is implemented. By designing a Johnson counter and Ring counter we have proved that the counter designed with pulse enhancement scheme provides low power consumption in the counters. The power consumption varies for different frequencies[4]. For any frequency, the pulse enhancement flip-flop shows reduced power consumption compared to other designs. By using a low power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 presacler based on pulse swallow topology dynamic logic multiband flexible integer-n divider can be proposed, the divider also uses low power loadable bit-cell for ring counter.

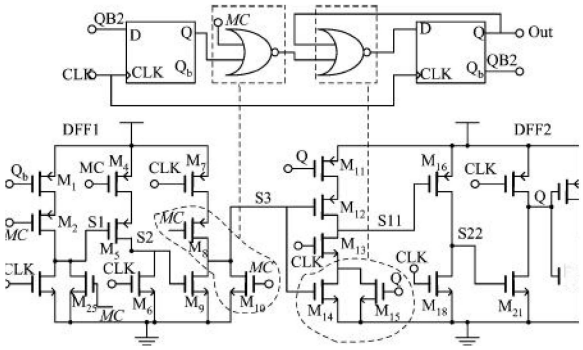

Fig.2. Wideband Single phase Clock 2/3 Prescaler.

Fig 2 represents the block diagram for 2/3 prescaler that incorporates two D flip flops and two NOR gates. The connections are made such that the output of first D flip flop is given as one of the input of first NOR gate, whose out is then fed to one input of second NOR gate. Now, output from this second NOR gate is applied to the input of second D flip flop. In certain conventional cases the load on DFF2 may limit the speed of operation and will also leads to power dissipation. Hence to overcome this problem above prescaler has been designed (fig 2) which consumes less power then conventional 2/3 prescaler and reduces the number of switching nodes from 12 to 7[5]. Hence it also reduces the area.

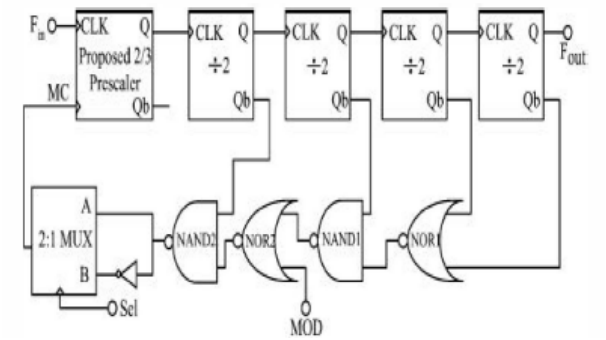

Fig 3 : Proposed multimodulus 32/33/47/48 Prescaler.

Fig.3 shows internal view of 32/33/47/48 Prescaler block, which consists of 2/3 prescaler, an asynchronous divider (div-by-16) and a control logic block which includes combination of NAND and NOR gates and a 2:1 multiplexer. Depending upon sel line wheather it is 0 or 1 the 32/33/47/48 prescaler can be implemented by using the following formulas,
When sel=0,

$$N = (AD * N1) = 32$$
$$N + 1 = ((AD - 1) * N1) + (1 * (N1 + 1)) = 33$$

When sel=1,

$$N = ((AD - 1) * (N1 + 1)) + (1 * N1) = 47$$
$$N + 1 = (AD * (N1 + 1)) = 48$$

Sel	MOD	MC	MODE
0	1	1	Divide-by-2
	0	1	Divide-by-2
	0	0	Divide-by-3
1	1	0	Divide-by-2
		1	Divide-by-3

TABLE 1: PRESCALER FREQUENCY DIVIDE RATIOS

ETSPC flip flops outstands TSPC flip flops, because of lower supply voltage and higher operating frequency .in divide-by-2 mode operation there will be redundant power consumption, hence to overcome this the control logic is changed from the output of first flip flop to its input. In TSPC the inverter between parallel connected transistor and both the flip flops may lead to larger parasitic capacitance with extra delay[6]. Hence , to prevent this problem, a new method is proposed using ETSPC technique as represented in fig 4. This is similar to TSPC, except that instead of two NOR gates an inverted AND gate and an pass transistor switch is used which overcomes the delay problem.

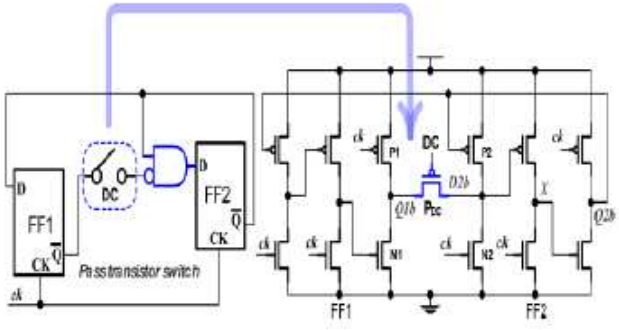

Fig 4: Circuit Diagram of E-TSPC based divide-by-2/3 prescaler.

Power consumption and propagation delay are the key factor for high speed digital circuits. The maximum operating frequency can be calculated as

$$fmax = \frac{1}{tpHL + tpLH}$$

The propagation delay of low to high transition is given by *t*pLH and high to low transition *t*pHL. The short circuit power

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and the switching power constitutes the total power that is consumed by the CMOS digital circuits. Hence, the short circuit power is described as the product of short circuit current and supply voltage as

$$PSC = ISC * Vdd$$

The switching power is described as the summation of product clock frequency supply voltage and load capacitance at output node of *i*th stage as

$$PSwitching = \sum f_{clk}\, cli\, vdd2$$

TSPC logic circuits has lesser short circuit power but higher switching power compared to E-TSPC logic circuits[7].Due to reduction in load capacitance, the E-TSPC when compared to TSPC has advantage of high operating frequency ,But short circuit power is the major disadvantage.

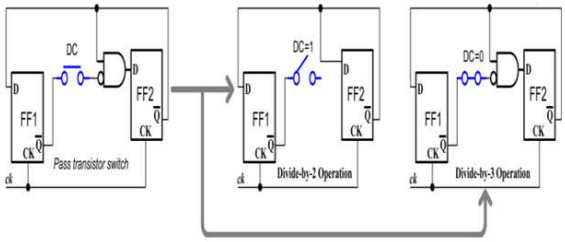


Fig 5: Logic structure of proposed divide-by-2/3counter design.

IV SIMULATION RESULTS

The proposed designs are simulated in Xilinx 14.7 and the outputs are shown below. Experimental results shows the power has been reduced with decrease in chip area .

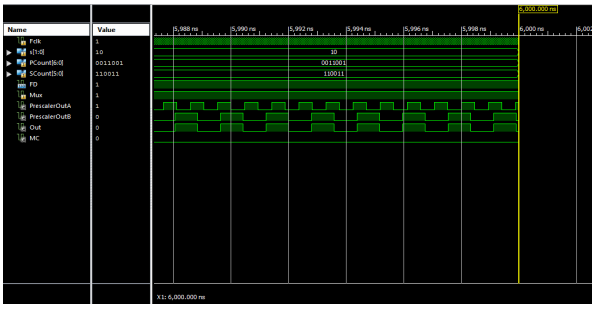


Fig 6: result when MC=0

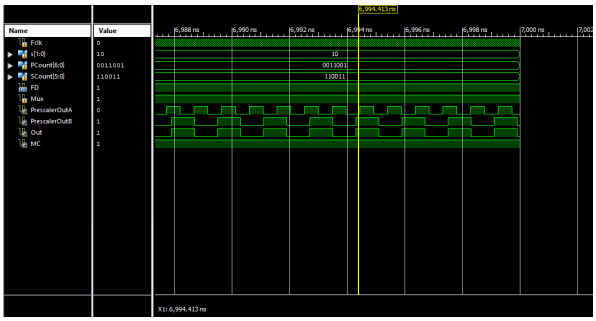
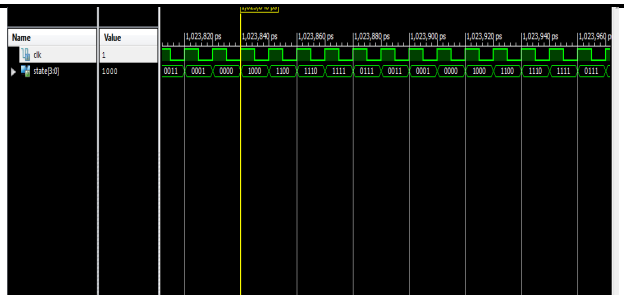


Fig 7: when MC=1



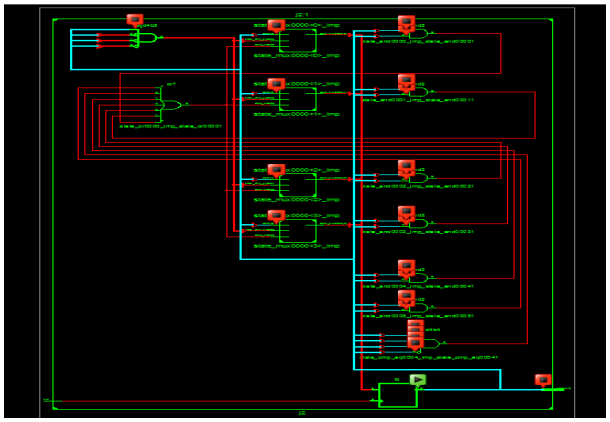
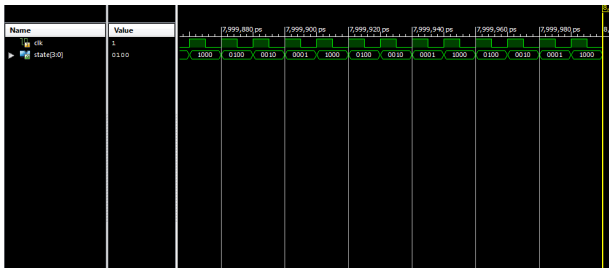


Fig 8: Johnson counter Result and RTL schematic



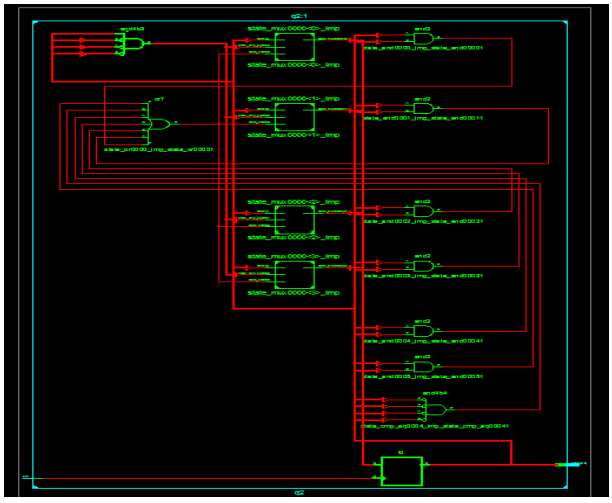


Fig 9: Ring counter Result and RTL schematic

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V .RESULTS AND COMPARISON

Design parameters	2004	2006	This work
Tech. (μm)	0.25	0.18	0.18
supply voltage (V)	1.8	1.8	1.8
Max.Freq(GHz)	6	6	6.5
Power(mW) Divide By 2 Mode	2.7	2.2	0.97
Power(mW) Divide by 3 Mode	6.25	2.62	1.78

Table 2: comparison table

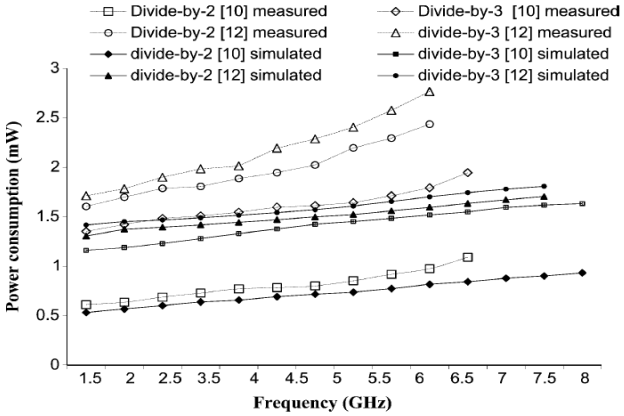

Fig 10: Post layout and measured power consumption results of 2/3 prescaler

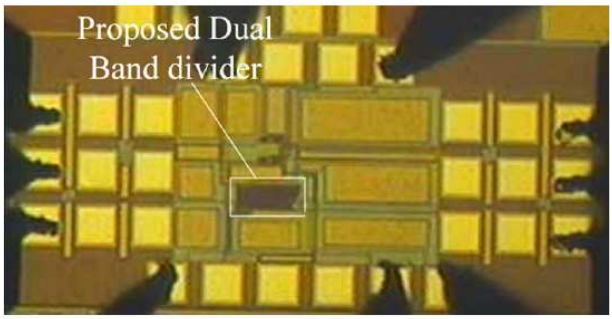

Fig. 11: Die photograph of the proposed multiband divider.

VI- CONCLUSION

In this paper the wireless local area network frequency synthesizer is presented for low power single phase clock distribution network. In this technique programmable and swallow counter is replaced by Johnson counter and ring counter respectively. By using such counters, the power consumption is reduced drastically and hence decreases the delay and area. Along with these counters the multimodulus prescaler is also used. . hence, with the help of multimodulus prescaler, the Clock Jitter can be removed.

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