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Power Efficient Parallel Adder Design Using CNTFET Technology

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***Abstract*- This paper presents the Power efficient Parallel Adder design using carbon nano tube field effect transistor. The ternary logic is a variable one as compared to the conventional binary logic design technique, because in the today's digital design it is possible to analyze energy efficiency and simplicity because the circuit has reduction in the chip area and interconnections. By using the load-resistive CNTFET ternary logic has designed to implement ternary logic which are based on the CNTFET, and is compared with the present resistive load CNTFET logic gate design. As, it is known to us that presented ternary logic gate technique design is combined with conventional binary gate technique design which have an excellent power consumption and speed characteristics in a circuits such as multiplier and full adder. By the simulation results using the SPICE technology the proposed ternary logic gates show the delay and low power comparing with the earlier resistive load CNTFET implementation, some of the new technologies in the CNTFET are, Fin-Field Effect Transistor, Single Electron Transistor and Silicon-On-Insulator.**

Index Terms: CNTFET (Carbon Nano Tube Field Effect Transistor), PDP (Power Delay Product), Parallel Adder, Ternary Digit.

INTRODUCTION

The alternative for the CMOS technology is the CNTFET. The similarity between CMOS and CNTFET in a device structure and principle operation, we can obtain the required CMOS manufacturing and CMOS design in the CNTFET technology. Some of the important characteristics of CNT are: high $\mathbf{I_{ON}/I_{OFF}}$ ratio, the unique dimension band which suppresses back scattering. Comparing CNTFET and MOSFET, MOSFET have more scalability and less size which makes them more suitable for displacing. Due to the excellent electric properties of CNTFET, the CNTFET are attractive for the nano electronic applications. The CNT's are high resistant to electro migration because the structure of a band is direct in which it enables the optical emission. Many of the efforts has been done to understand that how a CNT operates and how to improve the performance of transistor. All of the carbon bond atoms have well satisfied at the surface of carbon nano tube, which have a different semiconductor or oxide interface results. The carrier scattering mechanism and phonon vibration modes are little bit different in CNT which have different roles of phonon scattering in Carbon Nano Tube Field Effect Transistor. For the low power demanding arithmetic circuits the CNTFET's have low power consumption and high performance properties. The full adder cells are duplicated many times to build larger circuits.

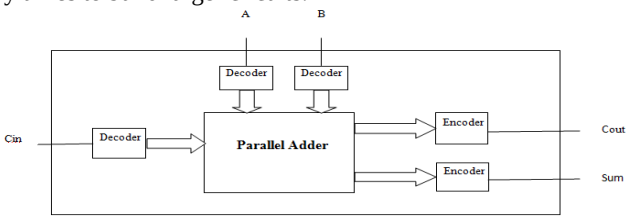

Fig1. General Block Diagram for the Proposed Technique

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	0	2

Table 1.1 Truth Table of Ternary Full Adder

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II.PREVIOUS WORK

K.Sridharan, Sundaraiah Gurindagunta, and Vikramkumar Pudi presented the design of single trit full adders and provide an extension to the multitrit full adders. An enhancement to the ternary single trit-full adder of [1] is presented in [2] with the advantage of speed-up. We focus on the one trit full-adder here since it constitutes the building block of the multidigit ternary full adder. The general structure of a three-trit full adder with three ternary inputs *A*, *B*, and *C*in and two ternary outputs *C*out and Sum as shown in fig.2

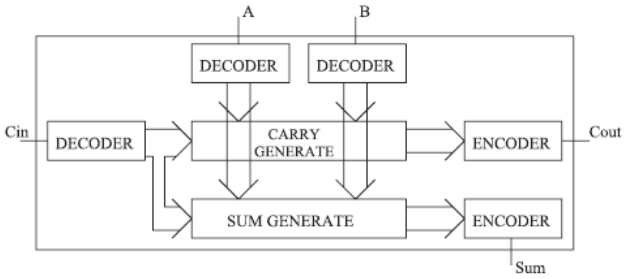

Fig 2: Block Diagram of Single trit adder

III. PROPOSED WORK

Here in the present paper the parallel adder is implemented using 4-bit carry look ahead adder ,in which it provides an extension for the CNTFET full adder extension i.e., for the single trit and multitrit full adders as presented in[1]. Fig 1 shows the general block diagram of the parallel adder, taking here an example of 4-bit adder.

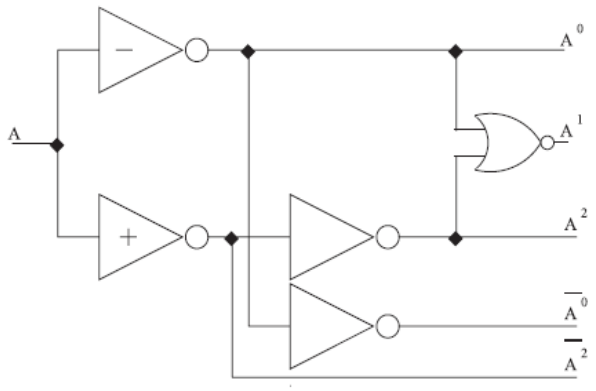

Fig 3.1: Decoder Circuit

Fig.3.1 shows internal view of decoder block, in this logic current input A is given to PTI (positive ternary inverter) and NTI (negative ternary inverter). The ternary decoder has, one input, three output combinational circuits and for an input A it generates unary functions. The decoder has one pti gate, two nti gates and one nor gate with it as shown in the above circuit.

$$\mathbf{A}_k = \begin{cases} 2, & \text{if } \mathrm{A} = k \\ 0, & \text{if } \mathrm{A} \neq k \end{cases}$$

Where the values of k are 0, 1 and 2.

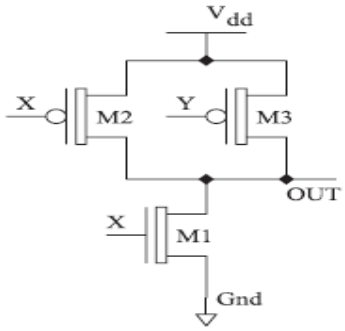

Fig3.2: Encoder Circuit

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Table 2.1 Truth Table for STI, PTI and NTI

The main function of encoder and decoder is that the encoder converts the binary values to the ternary, where as the decoder performs the ternary to the binary conversion for any of the circuit. The advantage of the ternary logic is it reduces the number of computations steps required. Each of the signals can have three different values; the total number of required digits in ternary is $\log_3 2$ times as with that of a binary logic as required. Therefore as by considering for an N bit binary adder the required ternary adder is $[\log_3 2N]$ digit value.

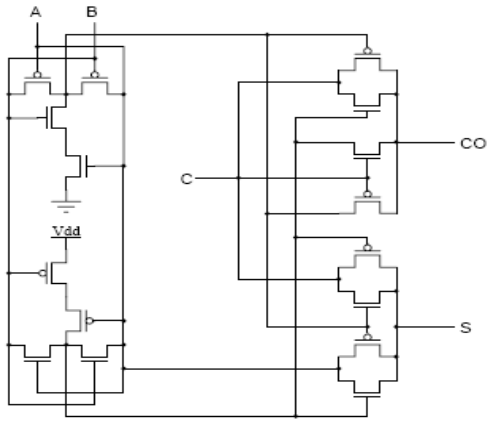

Fig 3.3: Circuit Diagram 16 Transistor Full adder

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Here a parallel adder is taken as an example for a full adder, with a 4-bit value and each single bit consists of 16 transistors as shown in fig 3.3 and which is presented in [1], it has total of 28 transistors. Here there are 16 transistors in each bit, and all the four bits are connected in parallel so as to perform sum and carry. In practical situations it is required to add two data each containing more than one bit. Two binary numbers each of *n* bits can be added by means of a full adder circuit. Consider the example that two 4-bit binary numbers B $_4$B $_3$B $_2$B $_1$ and A $_4$A $_3$A $_2$A $_1$ are to be added with a carry input C $_1$. This can be done by cascading four full adder circuits as shown in Figure 3.3. The least significant bits A $_1$, B $_1$, and C $_1$ are added to the produce sum output S $_1$ and carry output C $_2$. Carry output C $_2$ is then added to the next significant bits A $_2$ and B $_2$ producing sum output S $_2$ and carry output C $_3$. C $_3$ is then added to A $_3$ and B $_3$ and so on. Thus finally producing the four-bit sum output S $_4$S $_3$S $_2$S $_1$ and final carry output Cout.

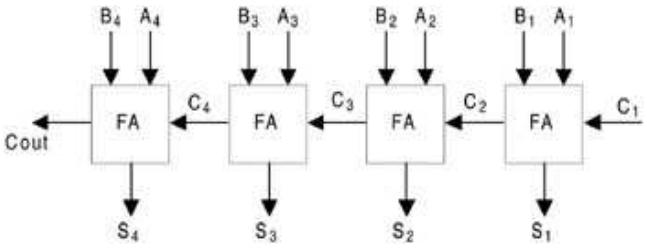

Fig 3.3: Cascading of four Full Adder Circuits

IV SIMULATION RESULTS

The proposed designs are simulated in H-Spice Simulation and Cosmo scope techniques and are shown in fig 4.1, 4.2, 4.3. Experimental results shows the logic resource utilization, delay, power parameters, area are efficient than previous methods.

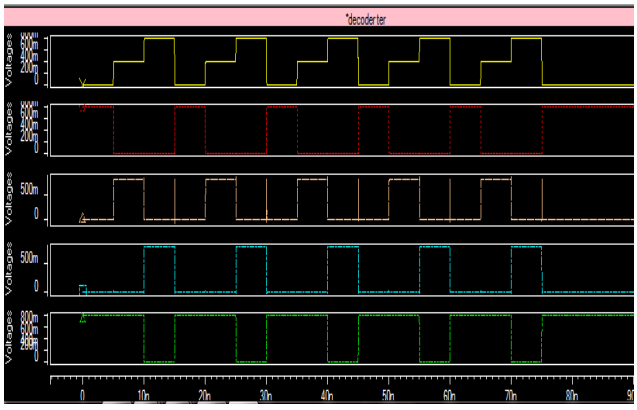

Fig 4.1 Decoder Simulation Result

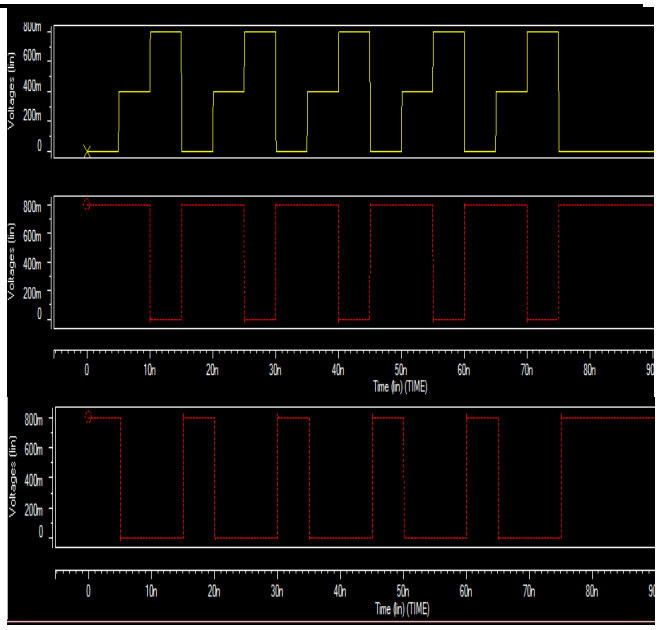

Fig 4.2 PTI and NTI simulation Result

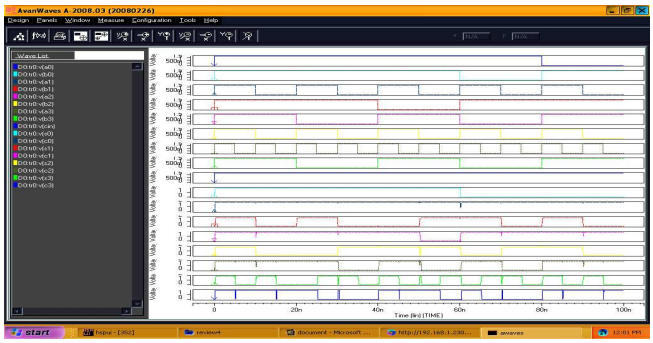

Fig4. Sum and Carry Simulation Result of Parallel Adder

V .RESULTS AND DISCUSSION

All the circuits mentioned above are compared with power, slew rate, rise time, fall time and delay and the parameters are more efficient than older method shown in table 5.1.Power estimation results are shown in fig 5.1, delay results are shown in fig 5.2. From results shown below we can conclude that proposed work results are efficient with respect to power, delay, and area than full adder technique. Here we represent the results of HSPICE simulation by using the MOSFET-like CNTFET model at 0.8 V power supply and room temperature. As the transient response of the proposed Single ternary adder is shown in Fig 2.The propagation delays have been measured from the change in input to the number of possible transitions of sum and carry outputs.

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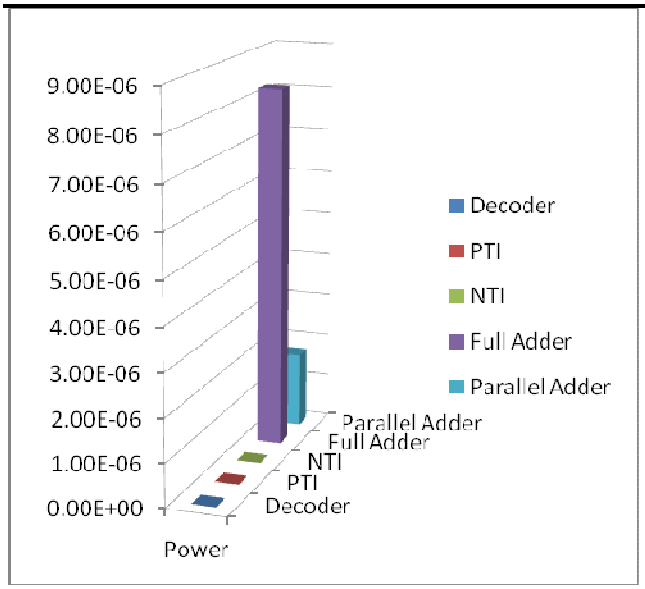

Fig 5.1: Power Dissipation (watts)

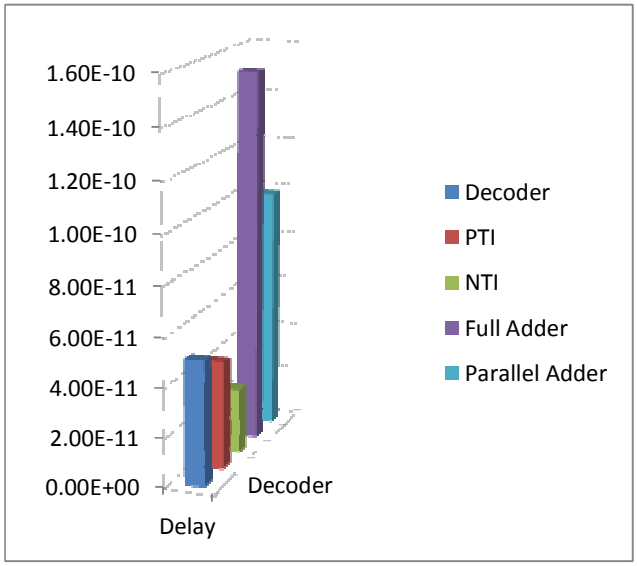

Fig 5.2: Delay (sec)

Parameters	Decoder	PTI	NTI	Full Adder	Parallel Adder
Power (watts)	28.70E-12	1.418E-15	25.53E-12	8.28E-6	17.2E-7
Delay (sec)	51.17E-12	44.13E-12	26.19E-12	152E-12	98.03E-12

Table 5.1: Comparison of Power and Delay

VI- CONCLUSION

In this paper the 4-bit full adder has implemented using the CNTFET technology. To perform the improvement in Full Adder circuit all the CNTFET's are used to activate the required guidance path which disables another path of the output. All the techniques are designed and simulated in H-Spice A-2008.03 and Cosmo cope tool. The design is based on the advanced ternary logic gates. It performs significant advantages in the reduction of the circuit complexity low power consumption and increased speed.

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