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Advanced Data Link Layer Techniques for Network on Chip Applications

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***Abstract*-Moore's law in VLSI technology making the designs more complex, which increases wirings in network on chip. Because of this there is power dissipation in data link of NoC. The main aim of this work is to reduce the coupling switching activity and self-switching activity of the data, these activities increase link power in NoC. The method works on end-to-end bases and the wormhole switching technique with pipelining. In this project encoder and decoder blocks are inserted in to network interface. It requires no changes in router design [3]. All data encoding schemes are designed in verilog HDL, synthesized in Xilinx 14.7, simulated in modelsim 6.3f.power estimation is done in Quartus II 9.1 simulated design software. Experimental results shows the resource utilization, frequency, delay, power parameters are efficient than existing methods. It reduces number of bit transition when data transits from 1 to 0 & 0 to 1.**

***Index Terms*-data encoding, network on chip, power estimation, switching activity.**

I. INTRODUCTION

Technology scaling makes system on chip designs more complex with more speed. Network-on-Chip (NoC) provides scaling of large number of processing elements and is best solution to many core designs [1]. Scaling provides speed advantage and making the designs more complex. Scaling in VLSI technology makes the design more complex and increase in power dissipation through data link layer in NoC [2]. The link layer elements includes network interfaces, routers etc.Proposed technique is shown in fig 1.1, it consists of routers, processing elements and network interface. Encoder and decoder block are inserted into network interface to reduce power consumption [3].

Table 1.1 shows transition activity of data before transmission and after transmission. There are four types of transitions as shown in table. Current data X that has to be transmitted is compared with previously encoded data Y. Based on this comparison decision for the inversion is done. The inversion technique used in this table reduces link power. In this work three encoding techniques are used to reduce the power consumption in network on chip links. These techniques reduce switching activity and hence reduce dynamic power. For any low power design signal activity has to be reduced when data transition takes from zero to one and one to zero.

In this work three encoding techniques; those are odd, even and full position encoding techniques are used to reduce switching activity [4].for all the techniques encoder and decoders are designed to implement proposed logic [3].

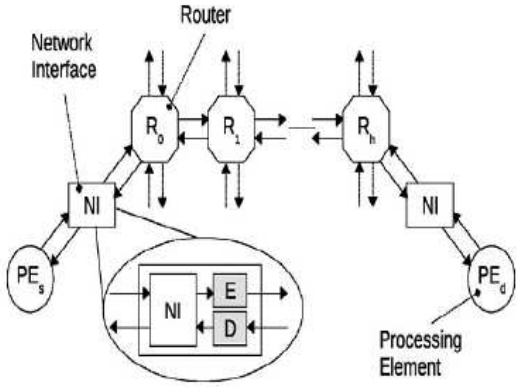

Fig 1.1 General Block diagram for proposed technique

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Table 1.1 odd inversion technique

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II.PREVIOUS WORK

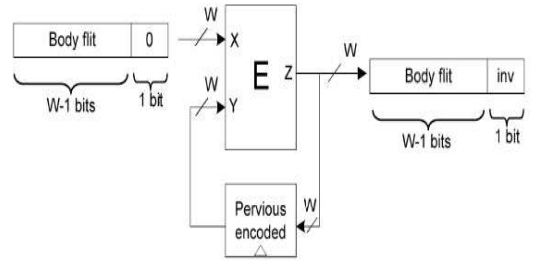
Invert encoding technique proposed in [2] uses odd inversion technique, in this work complexity is more, hence delay, logic element utilization and power consumption is more as compared to this work. The inversion technique used in previous work has more complexity that's why uses more interconnections. Power consumption in network on chip is reduced by coding techniques [4].

In this work three encoding techniques; those are odd, even and full position encoding techniques are used to reduce switching activity. For all the techniques encoder and decoders are designed to implement proposed logic .The method works on end-to-end bases and the wormhole switching technique with pipelining. In this project encoder and decoder blocks are inserted in to network interface. It requires no changes in router design [2].

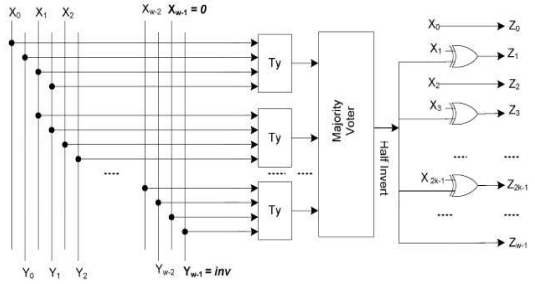
III.PROPOSED WORK

Technique-I

Fig 3.1(i) shows architecture for technique I data encoding. It consists of encoding logic block and is inserted into the network interface, the main function of this block is to decide whether inversion has to be done or not. It uses odd invert technique for link power reduction.



(i)



(ii)

Fig.3.1 Encoder design for encoding technique I. (i) block diagram (ii) Internal structure of E block.

Fig.3.1 (ii) shows internal view of encoder block, in this logic current data X that has to be transmitted is compared with previously encoded data Y. Based on this comparison decision for the inversion is done. Inversion action is indicated by inv bit. Data is inverted if inv=1, data is not inverted if inv=0.The ty blocks are used to detect transition types. The output of these blocks are given to majority voter, which sets output to high if any transition is detected, odd inversion is performed if output is high. Logic gates are used to perform odd inversion at the output. The inversion technique used in this method reduces link power. The decoder circuit simply inverts the received flit when the inversion bit is high.

Technique-II

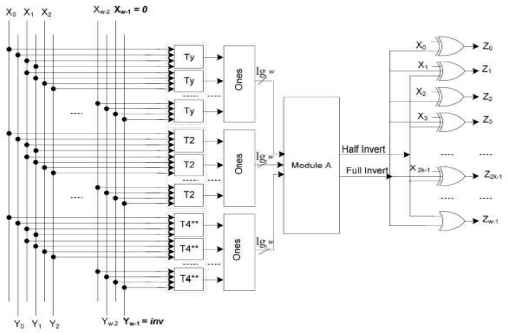
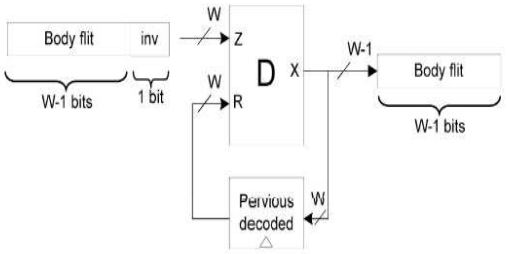
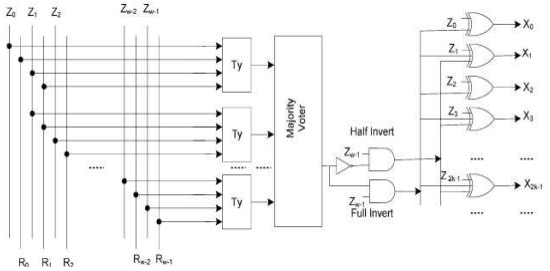


Fig 3.2 Encoder design for technique II

Fig 3.2 shows architecture for technique I data encoding. At very first the data which has to betransmitted is compared with previously encoded data.In fig first 1s block is used to identify the data which has to be odd inverted, middle 1s block is used to identify the data which has to be full inverted, last 1s block is used to identify the data which has to be even inverted.



i)



(ii)

Fig.3.3 Decoder design for technique II. (i) Block view. (ii) Internal structure of D block.

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Module A is used to decide which type of invert technique is applied to reduce power in data link. Inversion action is indicated by inv bit, data is odd or full inverted if inv=1, data is kept as it is if inv=0.Module A is designed using comparator and full adder blocks. Fig 3.3 shows architecture for technique II decoding. Incoming data is indicated by Z and R. Inversion action is indicated by inv bit. Data is inverted if inv=1, data is not inverted if inv=0.decoder uses Ty blocks to decide which invert method has to be applied. The output of the Ty block is applied to the majority voter, which decides particular invert method that has to be applied. For inv=1, if output is low half inversion is performed, if output is high full inversion is performed. The output of majority voter and logic gates are used to perform expected inversion.

Technique-III

Data encoding technique III use odd inversion, even inversion and full inversion. The encoded data bit is indicated by inv bit, encoder uses any one of the inversion method if inv=1, no inversion has been done, if inv=0.Encoder use Ty, Te, T2, T4** blocks. It also use 1s blocks to detect transitions. Module C is used to decide which inversion has to be performed. Logic gates are used to implement expected inversion techniques. Fig 3.4 shows Encoder design for technique III.

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

Table 3.1 Even inversion technique

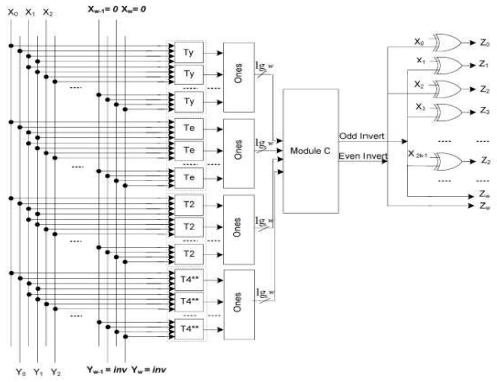

Fig 3.4 Encoder design for technique III

IV SIMULATION RESULTS

The proposed designs are simulated in Xilinx 14.7; Simulation results for all data encoding techniques are shown in fig 4.1, 4.2, 4.3. Experimental results shows the logic resource utilization, delay, power parameters are efficient than older method shown in table 4.1.

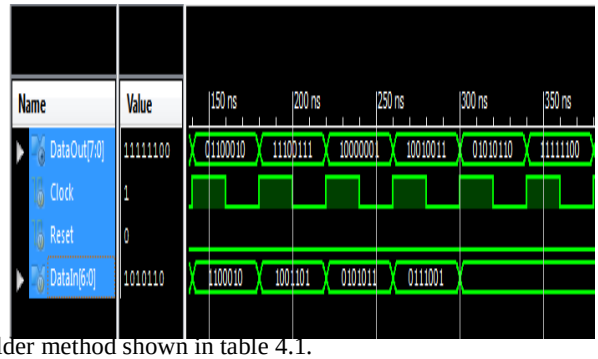

Fig 4.1 technique –I simulation Result

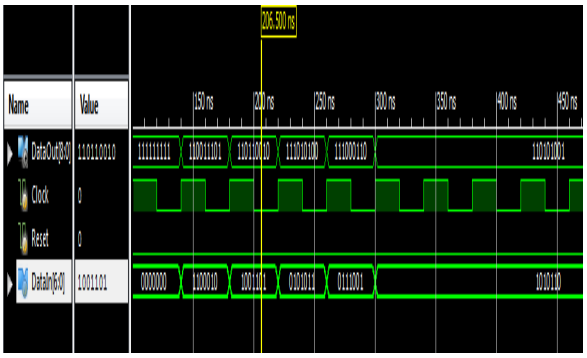

Fig 4.2 technique –II simulation Result

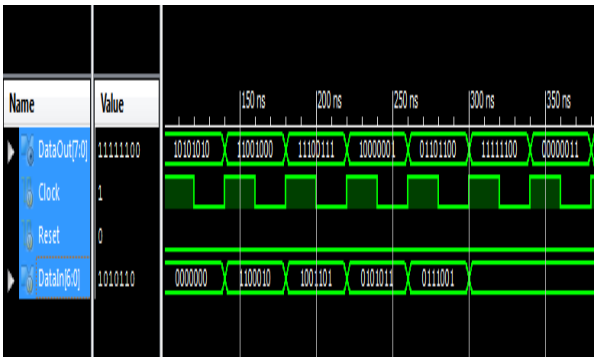

Fig 4.3 technique –III simulation Result

V .RESULTS AND DISCUSSION

Experimental results show the logic resource utilization, delay, power parameters are efficient than older method shown in table 5.1.Power estimation results are shown in fig 5.1, delay results are shown in fig 5.2, resource utilization is shown in fig 5.3.From results shown below we

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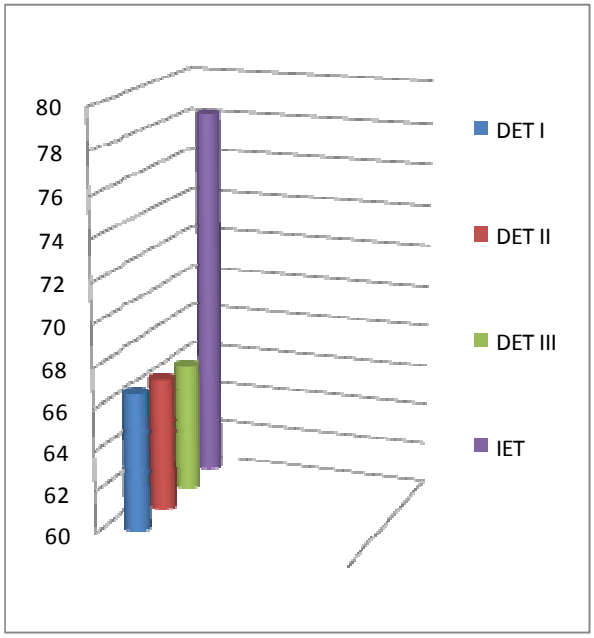
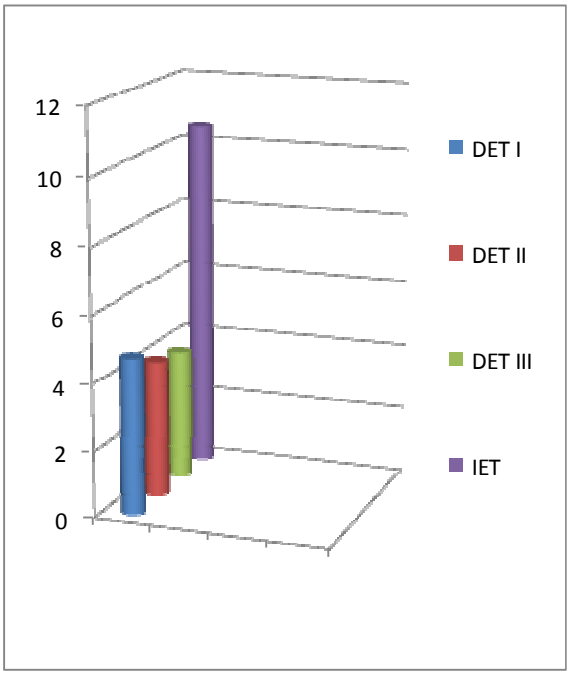
can conclude that proposed work results are efficient with respect to power, delay, resource utilization than invert encoding technique.



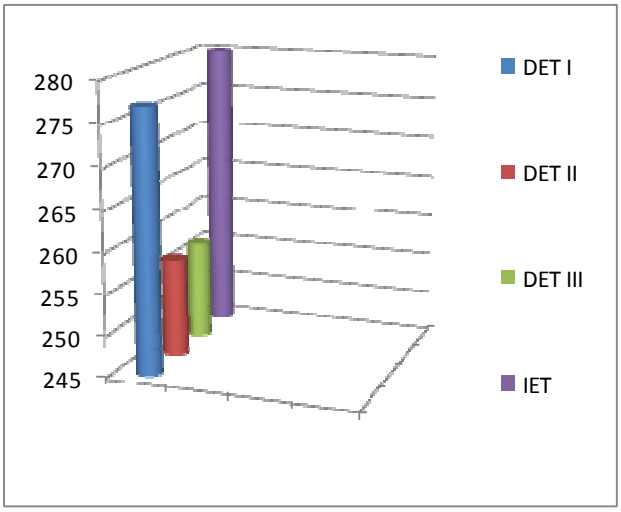
Power (mW)

Fig .5.1power estimation



Delay (ns)

Fig. 5.3 delay



Resource utilization (number of logic elements)

Fig. 5.2 resource utilization

METHODS USED	POWER	DELAY	LOGIC UTILIZATION(LOGIC ELEMENTS)
data encoding technique I	66.60 mw	4.706 ns	277 logic elements
data encoding technique II	66.50 mw	4.115 ns	257 logic elements
data encoding technique III	66.30 mw	3.928 ns	257 logic elements
invert encoding technique	78.16 mw	10.499 ns	280 logic elements

Table 5.1 Comparison for proposed data encoding techniques and invert encoding technique

VI- CONCLUSION

All data encoding techniques are designed in verilog HDL, synthesized in XILINX 14.7, simulated in MODELSIM 6.3F. Power estimation is done in QUARTUS II 9.1 design software**.** Experimental results shows the logic resource utilization, delay, power parameters are efficient than existing methods. It reduces number of bit transition when data transits from 1 to 0 & 0 to 1.

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