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Design and Analysis of NOC Torus Topology

VIKRAM
M.Tech Student (VLSI Design & Embedded System)
APPA Institute of Engineering & Technology
Kalburgi, Karnataka, India.
vikram.narboli09@gmail.com

ASSOCIATE PROF. RAKHA S
Dept. of Electronics & Communication Engineering
APPA Institute of Engineering & Technology
Kalburgi, Karnataka, India.
rekha_nl@yahoo.com

Abstract- Earlier **buses are used to connect from one processor to the processor. Due to the use of bus to connect from one processor to another there is delay in transfer of data to avoid delay and to reduce area. NOC topologies are used to connect from processing element to processing element. 2x2 torus and 5x5 mesh topology are designed and simulated in Xilinx 13.2 tool. NoC topology designed with 4 port router.**
***Index Terms*-torus topology, network on chip, mesh topology, 4 port router.**

I. INTRODUCTION

Communication between the processing element is done by the buses in the earlier days. Some of the processing element needs to communicate to another processing element to work efficiently therefore NoC topologies are used to connect one processing element to another processing element. NoC topology achieve inter process communication of processing element which will avoid using the bus .

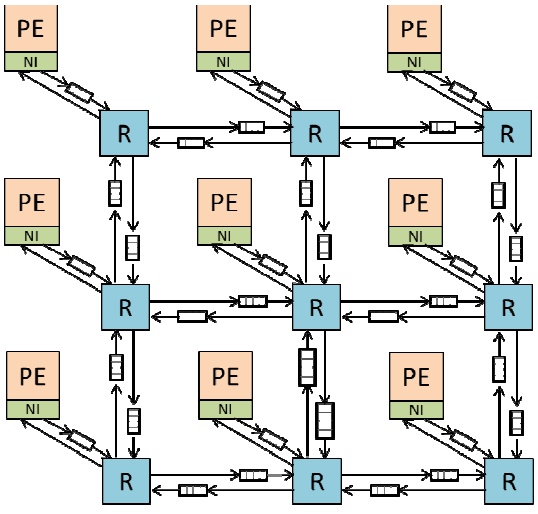

Fig 1 NoC architecture

NoC can be characterized by the structure of the routers connection, this structure or organization is called topology. NoC consist of 3 component links, router, and network adapter. Processing element with parallel communication requirement Buses may not produce required bandwidth latency and power consumption. A solution for such bottleneck is NoC**.** There are different topologies for the connection from one processor to another these are ring topology, line topology, star topology, mesh topology, torus topology. Grid topology. In ring topology processing element are connected in ring format. The drawback of using ring is if any processing element fails the packet is stopped to transfer from source to destination. In star topology all processing element are connected in star manner. To avoid deadlock condition we are using arbiter like round robin.

II. EXISTING METHODOLGY

Fig 2 Shows 5x5 Mesh topology consist of 25 processing element which are in the form of matrix format .Each processing element are connected by the 4 port router. 4 Port routers can transfer the data in 4 directions north, east,

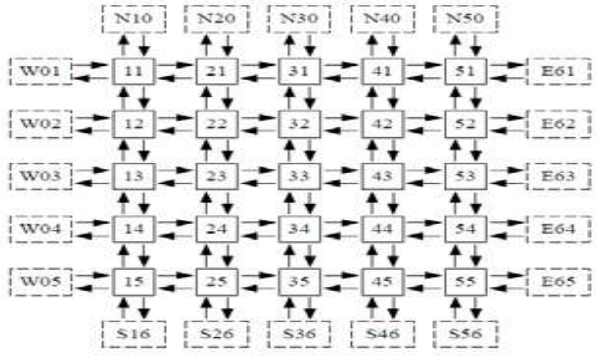

Fig 2 5x5 Mesh topology

west, south. Mainly router function to transfer the packet from source to the destination .Routing is done by the routing algorithm known as XY routing. Common routing algorithm are source routing and XY routing .In source routing the packet to be transferred is copied in processor then transmitted which consumes more time .In XY algorithm packet transmitted directly from source to destination by the packet follows the vertical first, then moves along the horizontal toward the destination or vice versa .For example if the packet to be transferred from processing element 11 to 55 the packet will be routed from row and column as follow 11,21,31,41,51,52,53,54,55 ,w01 to w05 and s16 to s56 and e61 to 65 and n10 to n50 are dummy tiles. This may be any processing element that connected to the processor .The advantage of using mesh and torus topology is that the date can be transmitted in 4 different paths. If any processing element is busy then data can be moved in different direction thus is not possible in other topology

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III PROPOSED METHODOLOGY

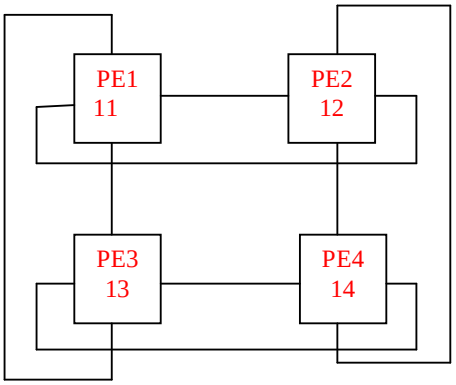


Fig 3 2x2 Torus topology

Fig 3 shows 2x2 torus topology which consist of 4 router which are connected to 4 processing element each router has 4 virtual channel totally there are 16 virtual channel to connect from one processing element to the another .Torus topology work efficiently to transfer the data compared to the mesh topology . .Data can be transferred from all the port .XY algorithm is used as routing topology to transfer the data from source to the destination

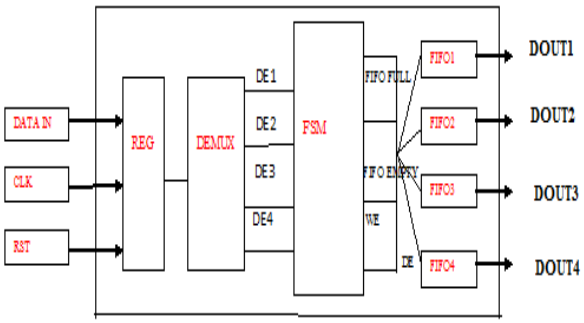


Fig 3.1: 4 Port router architecture

Fig 3.1 Shows 4 POURT router architecture it mainly .Consist of register to store the data input which depend upon whether clock is high or reset is low, 4:1 demultiplexer which takes 1 input and generate 4 output. The 4 outputs are DE1, DE2, DE3, DE4 the output flows to the input of FSM which act as controller the FSM check whether FSM is full or empty depending upon that the date is read and write.

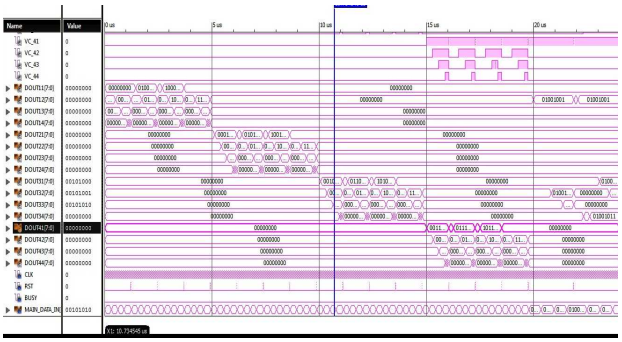
IV. SIMULATION RESULT

Table 4.1 Design summary of 5x5 mesh topology

mesh	used	available	utilization
No of slices	5764	14752	38%
No of slices flip flop	5844	29504	19%
No of luts	7782	29504	26%
No of bounded IOBS	4	24	16%

Table 4.2 Design summary of 2x2 torus topology

TORUS	used	available	utilization
No of slices	8542	14752	57%
No of slices flip flop	9077	29504	30%
No of luts	9589	29504	32%
No of bounded IOBS	17	24	70%



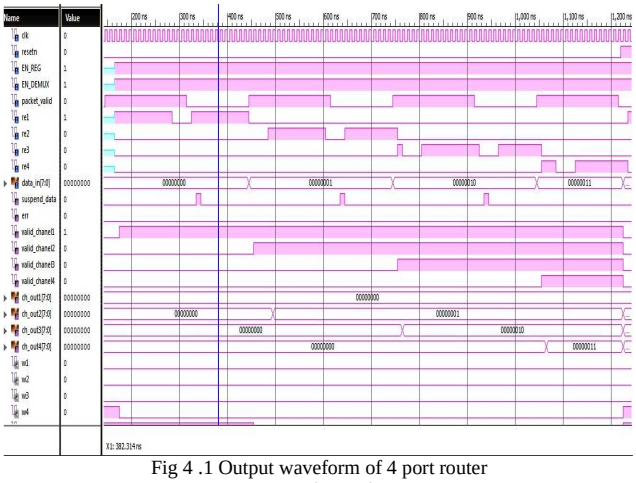


Fig 4 .1 Output waveform of 4 port router
Fig 4.2 Output waveform of torus topology

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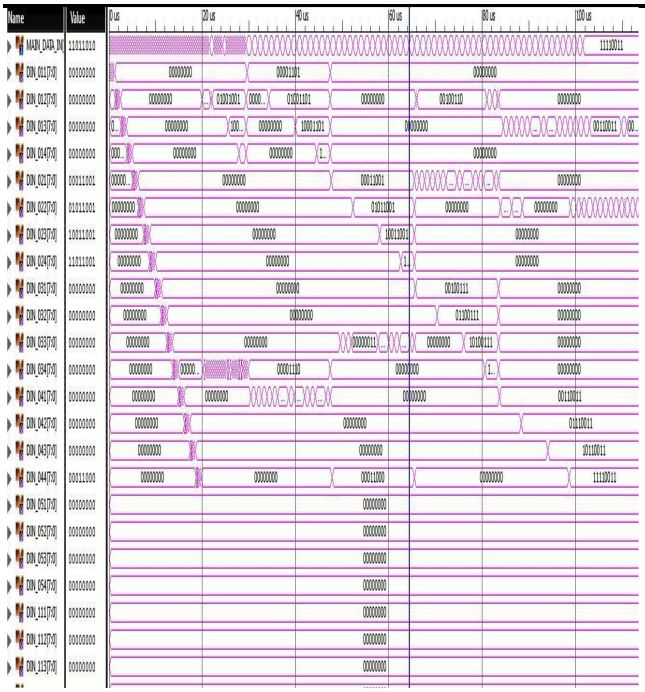

Fig 4.3 Output waveform 5x5 Mesh topology

IV CONCLUSION

Torus topology is designed in verilog HDL, simulated and synthesized in Xilinx 13.2. Experimental result show that purposed design has better resource utilization, memory utilization, and delay, than previous work.

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