International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 3, March 2015)

Design of Low Power Digital to Analog (DAC) Converter Using Mentor Graphics

Vatsala S.Bannikatti
MTech Student (VLSI Design & Embedded System)
AIET, Gulbarga, Karnataka, India
sbvatsala@gmail.com

Associate Prof.Rekha S
Department of Electronics & Communication Engineering
AIET, Gulbarga, Karnataka, India
rekha_nl@yahoo.co.in

***Abstract*- Digital to Analog (DAC) is used to get analog voltage corresponding to input digital data in VLSI circuit design with greater integration levels. However, providing linear current and voltage outputs with the use of strictly CMOS devices presents the need for a low power operational amplifier (op-amp) circuit. In this paper, the analysis of op-amp circuit for 3-bit DAC and 5-bit DAC is illustrated. In order to reduce the power dissipation, weighted resistor is utilized in the proposed design. To design the op-amp circuit for 3-bit DAC and 5-bit DAC, the design has been implemented in Mentor Graphics 130nm CMOS process technology.**

Keywords- CMOS, DAC, op-amp, weighted resistor, Mentor Graphics tool, 130nm Technology.

I.INTRODUCTION

The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are the data converters those are not only used for conversion of audio via microphone or loudspeakers, video via camera or display, into information that the computer or digital signal processor (DSP) can handle. In Fig1 illustrate the concept of the interfacing ADC and DAC between the analog and digital domains. The data converters are also used for data transmission via a channel, where the channel is either wire line or wireless (radio). Typically, the data (signal) is modulated onto a carrier according to some scheme. The signal is then sent over the channel with the carrier. The receiver will demodulate and extract the data (signal). The modulation can be done in both the digital and analog domain dependent on application and feasibility. The purpose of the Digital to Analog converter (DAC) is to transform the digital representation (input word) of a signal into its corresponding analog representation.

Digital-to-Analog Converter (DAC): It is a device for converting a digital usually binary code to analog signal (current, voltage or charges).The DAC acts as an interface between digital world and analog real world. The DAC inputs a digital signal and outputs an analog signal in form of current, voltages or charges.Fig2 shows the basic symbol for a DAC.

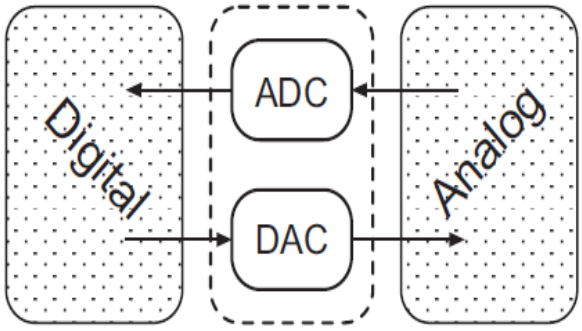


Fig1. Data converters as interface between the analog and digital domain

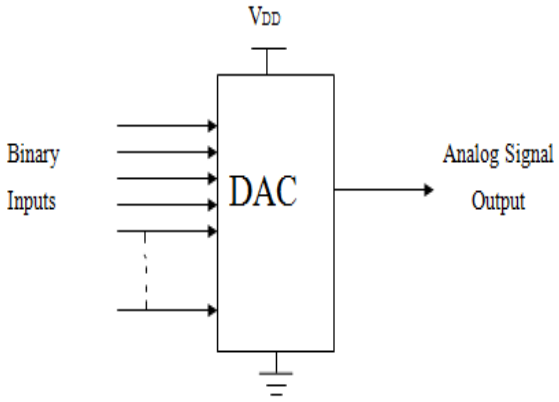


Fig 2. Symbol of DAC

II. PROPOSED METHODOLOGY

The proposed DAC design is based on conventional circuit of weighted summing amplifier as shown in Fig.3 Though, the op-amp is designed for ADC design implementation, but in this research, the design method is followed to use it in DAC structure without capacitor and current with high voltage and low power consumption . From the schematic diagram it is shown that, M1, M2, M3 are PMOS transistors with the W/L = 2 µm/0.13 µm. On the other hand, M4, M5, M6, M7 and M8 are NMOS with the W/L = 2 µm/0.13 µm. In the schematic diagram, M4 is connected to Input Negative

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 3, March 2015)

(INN) and M5 is connected to Input Positive (INP). Drain of M3 and M6 is connected to VOUT of the schematic.

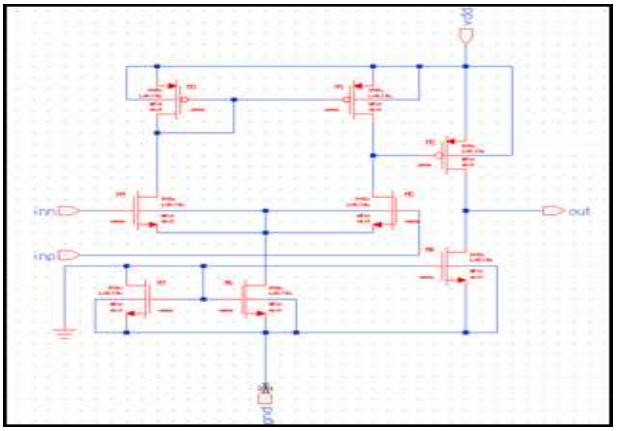


Fig 3. Schematic of low power opamp

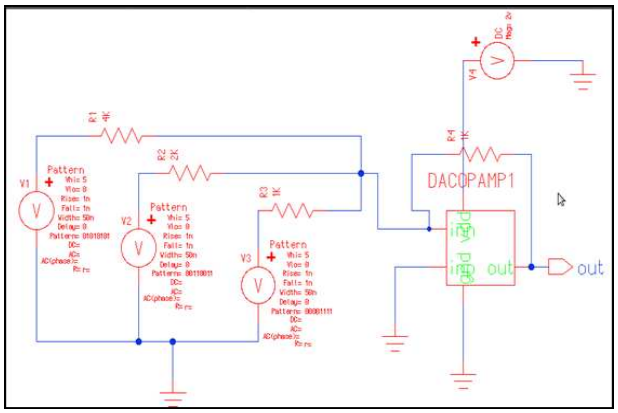


Fig 4. 3-bit DAC test circuit

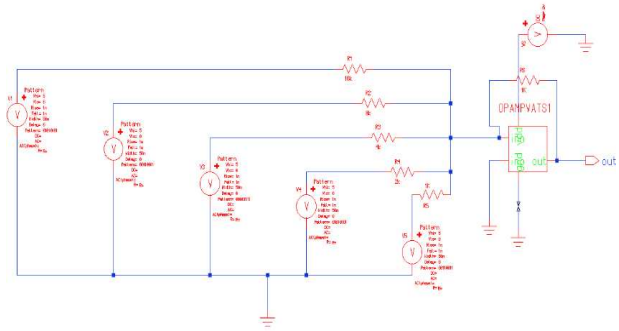
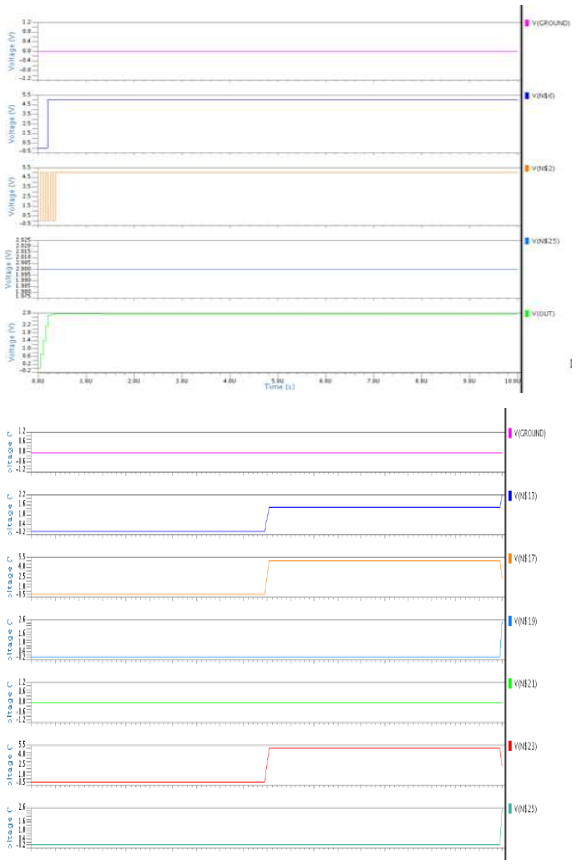
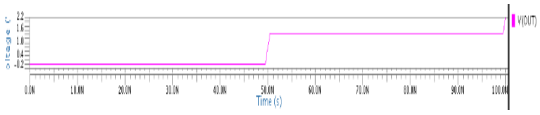


Fig5. 5-bit DAC test circuit

III. SIMULATION RESULTS



Simulation of 3-bit DAC



Simulation of 5-bit DAC

```
***** SYSTEM INFORMATION ...

*** User   : aiet@pc6
*** OS     : Red Hat Enterprise Linux Server release 6.0
*** CPU    :
    Pentium(R) Dual-Core  CPU      E5300  @ 2.60GHz
    Number of physical processors     : 1
    Hyper-Threading Technology        : disabled
    Number of cpu cores               : 1
    Number of logical processors      : 1
*** Freq   : 2600.000MHz
*** Cache  : 2048 KB
*** MEM    : 2060880 kB
*** Date   : Sat Feb  7 04:02:06 2015
```

Memory Usage

IV. CONCLUSION

The 3-Bit and 5-bit weighted resistor DAC circuit has been designed by using the Mentor graphics 130nm CMOS process technology.

From the above simulation results, the proposed design of digital to analog converter (DAC) has low power & high speed with high performance.

ACKNOWLEDGEMENT

I thankful to his Holiness Poojya Dr. Sharanabaswappa Appa, Mahadasoha Peethadhipati, Sharanabasaweshwar Samsthana, Gulbarga. President, Sharanabasaweshwar Vidhya Vardhak Sangha, Gulbarga.And also thankful to Principal, Dean AIET Gulbarga.

REFERENCES

[1]. Matthias Frey et al, "On the Static Resolution of Digitally Corrected Analog-to-Digital and Digital-to-Analog Converters with Low-Precision Components" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 54, NO. 1, JANUARY 2007.

[2]. Ankit Upadhyay et al, "3-bit R-2R Digital to Analog Converter with Better INL&DNL" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-2, Issue-3, February 2013.

[3]. Jurgen Deveugele et al, "A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 2, FEBRUARY 2006.

[4]. Kumar Parthasarathy et al, "A 16-bit Resistor String DAC with Full-Calibration at Final Test" 2005 IEEE.

[5]. Gaurav Raja et al, "16-bit Segmented Type Current Steering DAC for Video Applications" Proceedings of the 19th International Conference on VLSI Design (VLSID'06) © 2006 IEEE.

[6]. Nagendra Krishnapura "Efficient Determination of Feedback DAC Errors for Digital Correction in DS A/D converters" 2010 IEEE.