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POWER EFFICIENT BILBO DESIGN USING MENTOR GRAPHICS

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***Abstract*— This paper enumerates low power design of BILBO (Built-In-Logic-Block-Observer) using 5T-TSPC (MTCMOS) clocked latch. Latches are basic building block to design the BILBO. The clocked latches consume more power in the total power consumption of the BILBO. The power efficient 5TTSPC (MTCMOS) clocked latch is designed from the Basic 5T-TSPC clocked latch. The BILBO is designed by using both Basic 5T-TSPC clocked latch and 5T-TSPC (MTCMOS) clocked latch. The design of BILBO by using 5TTSPC (MTCMOS) consumes less power. The performance of BILBO is analyzed in terms of Number of Transistors (NT), Number of Clocked Transistors (NC) in Mentor Graphics 130nm technology.**

***Keywords*—TSPC, MTCMOS Technique, Mentor Graphics 130nm technology.**

I. INTRODUCTION

A. Clocked latch the combination of combinational circuit and memory element is called sequential circuit. Latch or Flip-flop is a memory element in sequential circuit. In a sequential circuit the memory element is required to know what has happened in the past. Flip-flop (Clocked latch) and latch is a circuit that has two stable states and can be used to store state information. The latch with the additional control input is called Clocked latch (Flip-flop).The additional control input is called clock. The clock provides the time reference point determine the movement of data in a digital system. The clocked latch is a basic building block to design any clocking system. The clocking system consists of a clock distribution network and clocked latch. The designed of clocked latch is crucial for the design of low power circuits as a digital block contains many memory elements. A large portion of the on chip power is consumed by the clocking system. The total power consumption of the clocking system depends on both clock distribution network and clocked latches (Flip-flops).The power consumption of clocked latch is higher than that of the clocking distribution network. The clocked latch is defined as "leading edge triggered". When the transition of the clock from 0-to1, the output (Q) is produced the same value of input (D).Conversely in a "negative edge triggered clocked latch". It is also possible to build a "double edge triggered clocked latch", that responds to both leading edge and trailing edge of the clock 'C'.

1) BILBO (Built-In-Logic-Block-Observer) is one of the BIST architecture.
2) BIST

BIST stands for Built-In-Self-Test. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside the chip. This increases the controllability and observability of the chip. Controllability is the ability to set (to1) and reset (to 0) every node internal to the circuit. Observability is the ability to observe either directly or indirectly the state of any node in the circuit. This makes the test generation and fault detection is easy. In BIST, the test generation and the output response evaluation are done in chip. A basic BIST configuration is shown in Fig 1. The main function of the test pattern generator is to apply test patterns to the unit under test. The resulting output pattern is transferred to the output response analyzer. A BIST scheme should be easy to important and must provide high fault coverage. BILBO has become one of the most widely technique for self testing of complex digital IC's.This technique is based on grouping the storage elements of the circuit; the method of incorporating a Built-In-Self-Test module is to use signature analysis or cyclic redundancy checking. A signature analyzer is constructed by cyclically adding the outputs of a circuit to the shift register if successive logic blocks are to be tested. Signature analysis can be merged With the scan technique to create a structure know as BILBO for Built-In-Logic Block Observation. It uses multipurpose module, called BILBO, that can be configured as function as an input test pattern generator or an output signature analyzer. This is composed of a row of Clocked latches and feedback operation.

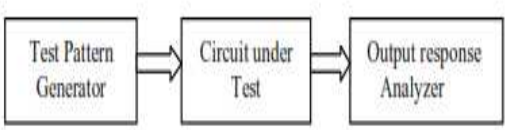

Fig 1. BIST configuration

Fig 2 shows logic diagram of a BILBO. The two control inputs B1 and B2 are used to select one of the four function modes.

1. **Mode 1:**B1=0, B2=1, All clocked latches are reset.

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2. **Mode2:B1**=1, B2=1, The BILBO behaves are latch. The input x1, x2, and x3 can be simultaneously clocked into the clocked latches and can be read from the Q and output.

3. Mode 3: B1=0,B2=0 the BILBO act as a serial SR. Data are serially clocked into the register through Sin, while the register contents can be simultaneously read at the parallel Q and Q outputs or clocked out through the Sout.

4. Mode 4:B1=1, B2=0, The BILBO is converted into a MISR. In this mode, it may used for performing parallel signature analysis or for generating pseudorandom sequences.

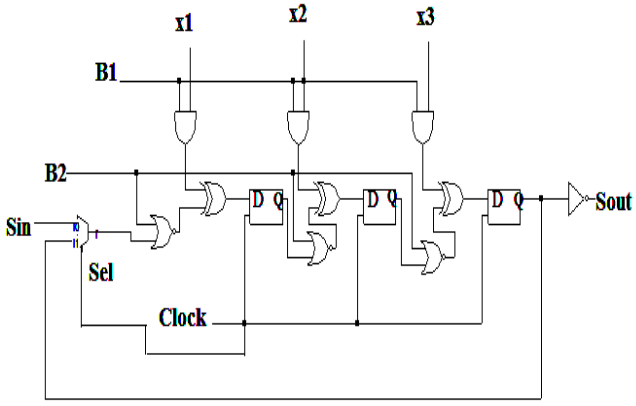

Fig 2. Logic diagram of a BILBO

II. PROPOSED METHODOLOGY

The proposed BILBO is designed by using 5T-TSPC (MTCMOS) clocked latch. The MTCMOS is introduced for reducing the power consumption. The MTCMOS technique is implemented by sleep transistors. The proposed block diagram is shown in fig 3.

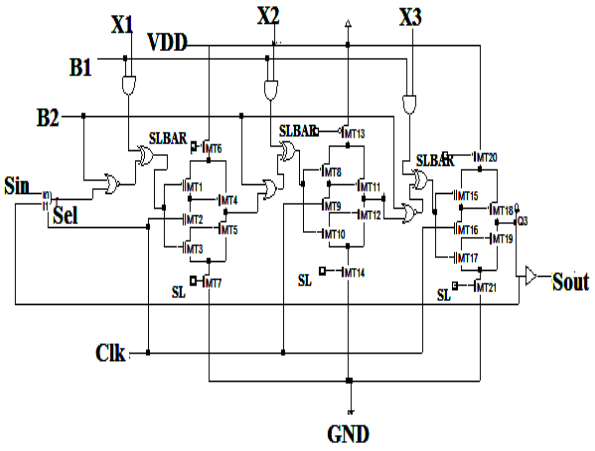

Fig 3. Block diagram of BILBO design

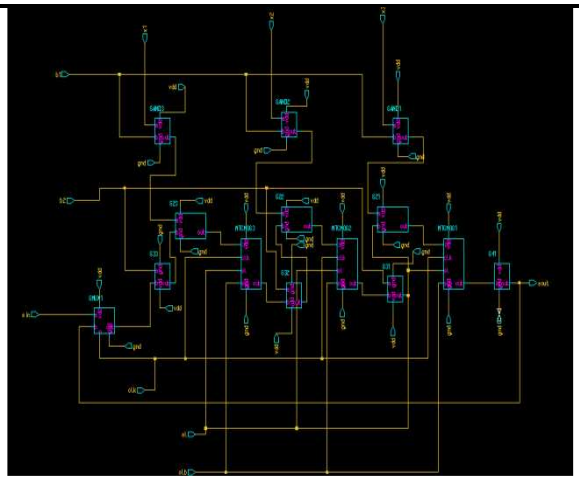

Fig 4. BILBO Design in Mentor Graphics

MTCMOS

Multi threshold CMOS (MTCMOS) is a variation of CMOS chip technology .The MTCMOS is implemented by use of sleep transistors for reducing power. Logic is supplied by virtual power rail. Low Vth devices are used in the logic where fast switching, speed is important. High Vth devices connecting the power rails are turned ON in active mode, OFF in sleep mode. High Vth devices are as sleep transistors to reduce the static leakage power. The multi threshold voltage (MTCMOS) circuit was proposed by inserting high threshold devices in series into low –Vthcircuitry. The schematic of 5T-TSPC (MTCMOS) clocked latch is shown in Fig 5. A sleep control scheme is introduced for efficient power management. During regular mode of operation, the extra transistor is turned on. This provides substantial savings in leakage current during standby mode of operation.

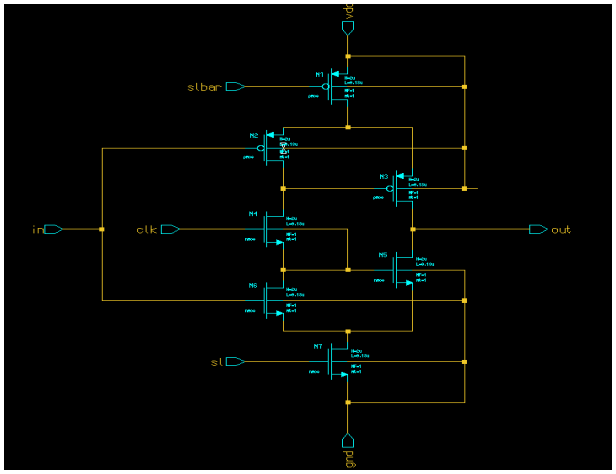

Fig 5. Schematic of 5T-TSPC (MTCMOS)

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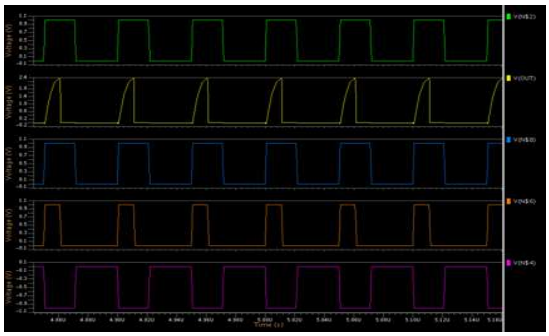
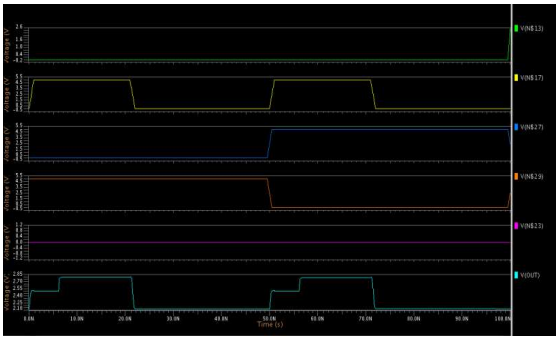
III. SIMULATION RESULTS

a. Simulation result of BILBO in Mentor Graphics



b. Simulation result of 5T-TSPC MTCMOS



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SIMULATION INFORMATION
memory size allocated in Mbytes  94.96
nb of components: 295
nb of nodes: 254
nb of MOS or BIP calls: 27770
Number of steps computed: 0

***>CPU TIME 0s 090ms <***

Searching Operating Point between -1.000000e+13V and
                                  1.000000e+13V

--> Partitioning circuit...

***> DC CPU TIME 0s 010ms <***

DC:7 iterations FOR DC analysis

   TOTAL POWER DISSIPATION:  7.0502M     WATTS
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Power Details

IV. CONCLUSION

From the simulation results it is concluded that the 5T-TSPC (MTCMOS) clocked latch consumes less power 7.0502mw than the Basic 5T-TSPC clocked latch. By applying MTCMOS technology the power is reduced. The proposed design circuit has been designed by using the Mentor graphics 130nm CMOS process.

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