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Transient Stability Improvement in Power System in Multi Machine System with Robust Distributed Static Series Compensator - A Review

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Abstract— **This paper is highlighting review of improvement the transient stability of the power system with the utilization of robust Distributed Static Series Compensator (DSSC) in transmission line power flow control. DSSC has operated similarly as a Static Synchronous Series Compensator (SSSC) but is in smaller in size and lesser cost along with various other factors. Simulation results support the DSSC capability for improving transient stability boundary of the power system.**

The theory of DSSC is on the support of using a small power single-phase inverter, which connected to the transmission conductor and vigorously controls the consequent transfer impedance. Through this, the dynamic control of power flow in the line is attained. Therefore, the lowest degree of available and describe technical projects for DSSC conform further more studies on the other factors of this apparatus. This study serves a research where 1400 DSSCs are incorporate in a two-area, two-machine system in order to study the transient stability of the system. By the intend of improving the transient stability, a complementary controller have been considered and properly shared to the main control loop of DSSCs. Simulation results demonstrate the resourceful influence of DSSCs in the transient stability expansion.

***Index Terms*— Distributed Flexible AC Transmission System (D-FACTS), Voltage Source Inverters (VSI), Pulse Width Modulation (PWM), Distributed Static Series Compensator (DSSC), Transient Stability Enhancement.**

I. INTRODUCTION *(HEADING 1)*

In recent times new theories from the relations of Distributed FACTS (D-FACTS) have been established as a technique to overcome the most of severe margins of FACTS devices. D-FACTS devices suggest all capabilities of their FACTS counterparts. The distributed character of the recommended system makes it feasible to attain very well granularity in the system evaluation.

II. FACTS

Flexible AC Transmission Systems, called FACTS, got in the modern years a well known name for advanced controllability in power systems by means of power electronic devices. A number of FACTS-devices have been introduced for a variety of applications in worldwide. A number of new types of devices are in the period of being introduced in practice.

In most of the applications the controllability is utilized to avoid cost intensive or landscape requiring extensions of power systems, for example like upgrades or additions of substations and power lines. FACTS-devices make available a superior variation to varying operational circumstances and improve the procedure of existing installations. The fundamental applications of FACTS-devices are: Power flow control, Increase of transmission capability, Voltage control, Reactive power compensation, Stability improvement, Power quality improvement, Power conditioning, Flicker mitigation, Interconnection of renewable and distributed generation and storages.

Figure 1 represents the fundamental proposal of FACTS for transmission systems. The handling of lines for active power transmission should be perfectly up to the thermal confines. Voltage and stability confines should be shifted with the way of the more than a few dissimilar FACTS devices. It can be seen that with rising line duration, the occasion for FACTS devices gets more additional important.

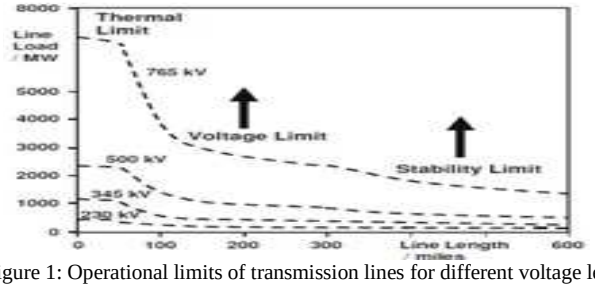

Figure 1: Operational limits of transmission lines for different voltage levels

The improvement of FACTS-devices has happening with the increase capabilities of power electronic apparatus. Apparatus for elevated power levels has been prepared presented in converters for high and still highest voltage levels. The overall opening points are network essentials impact the reactive power or the impedance of a component of the power system. Figure 2 represents a number of fundamental apparatus divided into the conservative ones and the FACTS-devices.

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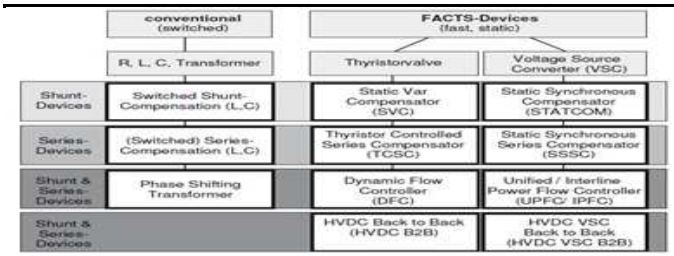

Figure 2: Overview of major FACTS-Devices

The main drawback is that with a growing switching frequency, the losses are growing as well. Consequently particular create of the converters are mandatory to recompense this.

III. Distributed Static Series Compensator (DSSC)

In recent times, latest theories from the relations of Distributed FACTS (D-FACTS) have been establishes as a technique to eliminate these barriers. The distributed environment of the recommended arrangement makes it achievable to accomplish excellent granularity in the system evaluation. Furthermore, it is achievable to enlarge the arrangement with the increasing require. This provides a significant advantage in development the arrangement, which permits the schemer to have managed on Existing Transfer Capability (ETC). It is completed in a technique that the increasing requirements in power transfer are fulfilled by providing innovative D-FACTS devices in the line for 15 years; this is finished in order to assemble project development requirements without having to invest the entire principal at the start of the project accomplishment.

The theory of Distributed Static Series Compensator (DSSC) is derived from the utilization of a low-power single-phase inverter, which joins to the transmission conductor and energetically controls the impedance of the transmission line, providing the organization of active power flow on the line. The DSSC theory gets over most of the severe restrictions of FACTS devices and designates the technique to an innovative approach for getting the power flow control.

DSSC has been in recent times projected to get over SSSC's difficulties. The most important difficulty in extensive applications of SSSC and further FACTS controllers include the non-promotable capability of the system produce to elevated investment at once, pricey elevated-rated power electronics, permanent maintenance and time consuming renovate. The extend character of the DSSC system can get over that type of difficulties by changing the lumped and elevated power SSSC into a distributed system including plenty of low power counterbalance devices along with the equivalent whole quantity of counterbalance. Figure 3 represents the DSSC distributed components.

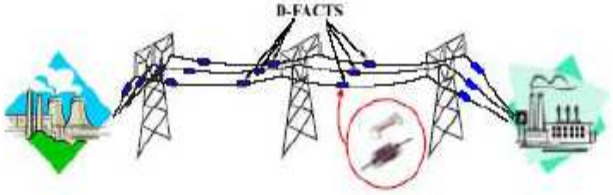

Figure 3: Distributed compensation system

IV. DSSC Simulate

A. Operating Principles of DSSC

A DSSC component, which is in series-connected with the transmission line all the way through the coaxial transformer, introduces a self-governing leading or lagging voltage with respect to the line current consecutively to control the power flow of the line.

In this regard, a single DSSC component acts just like a SSSC components. Figure 4 represents SSSC operation principals. Let us assume that a counterbalance component is joined to bus *j* and controls the power flow of line *j-i*. This figure 4 is as well alike for a DSSC component operation and is applicable for DSSC simulating.

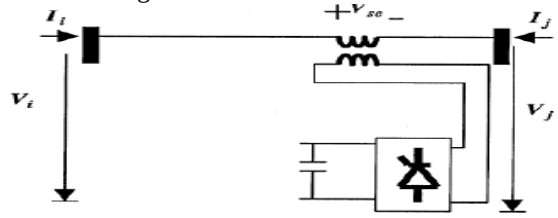

Figure 4: SSSC operation principles

B. Corresponding Circuit and Power Flow Constraints

DSSC simulating is founded on SSSC simulating along with two most important dissimilarities. Earliest, the DSSC components are located separately on system phases requiring a three-phase model and three-phase power flow as represented in Figure 5. The subsequent dissimilarity is the continuation of a number of components in a DSSC system distributed consistently all along the line. Taking into consideration all of these components in the model is not realistic, for that reason, it is understood that the counterbalancing system is having a three most important components every one comprising in excess of single component. These three components are located at the opening, center and the closing stages of the transmission line.

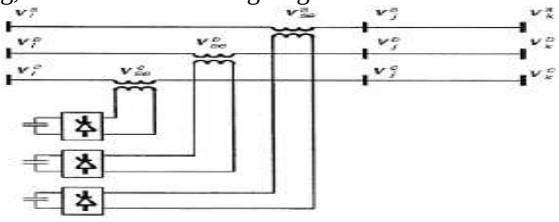
Figure 5: Three phase compensation

Similar to a SSSC, a DSSC component is as a self-governing voltage resource in series with transformer impedance. Figure 6 represents such a corresponding circuit acquires for every one phase correspondingly and separately.

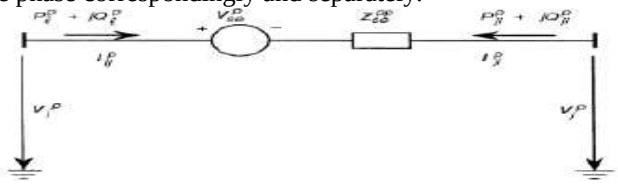
Figure 6: Single phase equivalent circuit

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If $V_{se}^{p} = V_{se}^{p} \angle\theta_{se}^{p}$, $V_{i}^{p} = V_{i}^{p} \angle\theta_{i}^{p}$ and $V_{j}^{p} = V_{j}^{p} \angle\theta_{j}^{p}$ subsequently the power flow constraints of DSSC components are:

$$P_{ij}^{p} = V_{i}^{p2} g_{ii}^{pp} - V_{i}^{p} V_{j}^{p} (g_{ij}^{pp} \cos(\theta_{i}^{p} - \theta_{j}^{p}) + b_{ij}^{pp} \sin(\theta_{i}^{p} - \theta_{j}^{p})) - V_{i}^{p} V_{se}^{p} (g_{ij}^{pp} \cos(\theta_{i}^{p} - \theta_{se}^{p}) + b_{ij}^{pp} \sin(\theta_{i}^{p} - \theta_{se}^{p})) \quad (1)$$

$$Q_{ij}^{p} = -V_{i}^{p2} b_{ii}^{pp} - V_{i}^{p} V_{j}^{p} (g_{ij}^{pp} \sin(\theta_{i}^{p} - \theta_{j}^{p}) - b_{ij}^{pp} \cos(\theta_{i}^{p} - \theta_{j}^{p})) - V_{i}^{p} V_{se}^{p} (g_{ij}^{pp} \sin(\theta_{i}^{p} - \theta_{se}^{p}) - b_{ij}^{pp} \cos(\theta_{i}^{p} - \theta_{se}^{p})) \quad (2)$$

$$P_{ji}^{p} = V_{j}^{p2} g_{jj}^{pp} - V_{i}^{p} V_{j}^{p} (g_{ij}^{pp} \cos(\theta_{j}^{p} - \theta_{i}^{p}) + b_{ij}^{pp} \sin(\theta_{j}^{p} - \theta_{i}^{p})) + V_{j}^{p} V_{se}^{p} (g_{ij}^{pp} \cos(\theta_{j}^{p} - \theta_{se}^{p}) + b_{ij}^{pp} \sin(\theta_{j}^{p} - \theta_{se}^{p})) \quad (3)$$

$$Q_{ji}^{p} = -V_{j}^{p2} b_{ii}^{pp} - V_{i}^{p} V_{j}^{p} (g_{ij}^{pp} \sin(\theta_{j}^{p} - \theta_{i}^{p}) - b_{ij}^{pp} \cos(\theta_{j}^{p} - \theta_{i}^{p})) + V_{j}^{p} V_{se}^{p} (g_{ij}^{pp} \sin(\theta_{j}^{p} - \theta_{se}^{p}) - b_{ij}^{pp} \cos(\theta_{j}^{p} - \theta_{se}^{p})) \quad (4)$$

Where $g_{ij}^{pp} + jb_{ij}^{pp} = \frac{1}{Z_{\omega}^{pp}}$, $g_{ii}^{pp} = g_{jj}^{pp} = g_{ij}^{pp}$, $b_{ii}^{pp} = b_{jj}^{pp} = b_{ij}^{pp}$ and *p* (*a*, *b* or *c*) shows line three phases.

With introducing the DSSC component keen on the system, two latest power constraints are required to explain for the component voltage amplitude and phase angle. The earliest constraint is the DSSC component zero active power replaces and the subsequent is the active power flow constraint of the counterbalancing line given by equation (5) and equation (6) respectively.

$$PE = \mathrm{Re}\{V_{se}^{p} I_{ji}^{p*}\} = 0$$

$$\mathrm{Re}\{V_{se}^{p} I_{ji}^{p*}\} = -V_{i}^{p} V_{se}^{p} (g_{ij}^{pp} \cos(\theta_{i}^{p} - \theta_{se}^{p}) - b_{ij}^{pp} \sin(\theta_{i}^{p} - \theta_{se}^{p})) + V_{j}^{p} V_{se}^{p} (g_{ij}^{pp} \cos(\theta_{j}^{p} - \theta_{se}^{p}) + b_{ij}^{pp} \sin(\theta_{j}^{p} - \theta_{se}^{p})) \quad (5)$$

$$P_{ji}^{p} - P_{ji}^{p,Spec} = 0 \quad (6)$$

V. Transient Stability Examination

Transient stability examine present information associated to the capacity of a power system to continue in synchronism for the duration of most important instability consequential from whichever the loss of originating or transmission conveniences, unexpected or continuous load variations, or temporary faults. Particularly, this type of studies make available the variations in the voltages, currents, powers, speeds, and torques of the machines of the power system, additionally as the variations in system voltages and power flows, for the duration of and instantaneously subsequent a trouble. The amount of stability of a power system is a significant aspect in the development of innovative conveniences. Consecutively to make available the dependability mandatory by the reliance on constant electric service, it is essential that power systems be considered to be stable under any feasible trouble.

A. Factors Influencing Transient Stability

- How greatly the generator is loaded.
- The generator output for the duration of the fault, this depends on the fault position and type.
- The fault reimbursement moment.
- The previous fault transmission system reactance.

B. Possibilities for Improving the Transient Stability boundary of a Power System

- Augment of system voltages, utilization of AVR.
- Utilization of elevated speed excitation systems.
- Decrease in system transfer reactance.

A transient stability examine is executed by joining a explanation of the algebraic equations describing the network with a numerical solution of the differential equations. The solutions of the network an equation sustain the characteristics of the system and by this means make available admission to system voltages and currents for the period of the transient period.

VI. Single-Phase Voltage Source Inverters

Single-phase Voltage Source Inverters (VSIs) can be establishing as half-bridge and full-bridge methods.

A. Half-Bridge Voltage Source Inverters

Figure 7 represents the power procedure of a half-bridge VSI, where two large capacitors are needed to make available a neutral point N, such that every single capacitor preserve a steady voltage v_i=2. For the reason that the current harmonics introduced by the procedure of the inverter are short-order harmonics, a set of large capacitors (C_+ and C_-) is needed. It is understandable that together switches (S_+ and S_-) cannot be on at the same time for the reason that a short circuit transversely the dc link voltage source v_i would be developed. There are two distinct (states 1 and state 2) and single indeterminate (state 3) switch state as represented in Table 1. In order to keep away from the short circuit transversely the dc bus and the indeterminate ac output voltage circumstance, the modulating procedure should for all the time make sure that at every instantaneous whichever the peak or the base switch of the inverter leg is on.

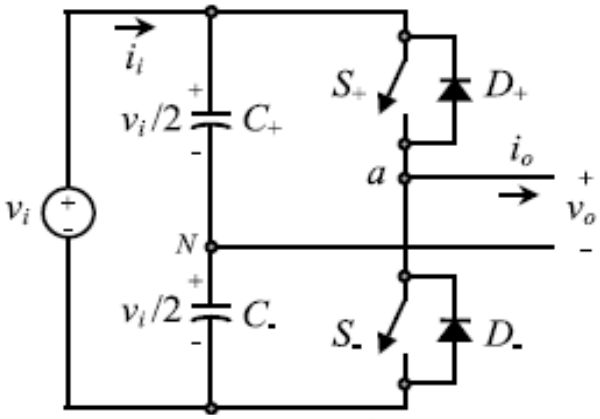

Figure 7: Single-phase Half-bridge VSI

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Table 1 Switch states for a Half-bridge single-phase VSI
VII. \

State	State	v	Components Conducting
$_+$ is on and $_-$ is off	1	$v/2$	$_+$ if >0
			$_+$ if <0
$_-$ is on and $_+$ is off	2	$-v/2$	$_-$ if >0
			$_-$ if <0
$_+$ and $_-$ are all off	3	$-v/2$	$_-$ if >0
		$v/2$	$_+$ if <0

Figure 8 represents the perfect waveforms connected with the Half-bridge inverter. The states for the switches S_+ and S_- are definite by the modulating procedure, which in this case is a carrier-based PWM.

Figure 8 evidently represents that the ac output voltage $v_o = v_{aN}$ is essentially a sinusoidal waveform along with harmonics, which features: the magnitude of the essential factor of the ac output voltage $\hat{v}_{o1}$ fulfilling the subsequent term $\hat{v}_{o1} = \hat{v}_{aN1} = \frac{v_i}{2} m_a$

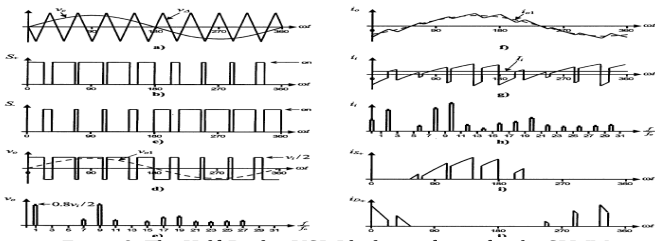

Figure 8: The Half-Bridge VSI. Ideal waveforms for the SPWM

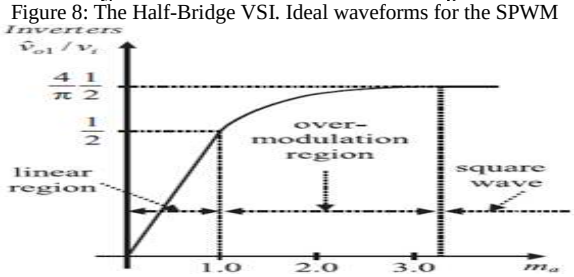

Figure 9 essential ac part of the output voltage in a Half-Bridge VSI SPWM modulated Full-Bridge Voltage Source Inverters

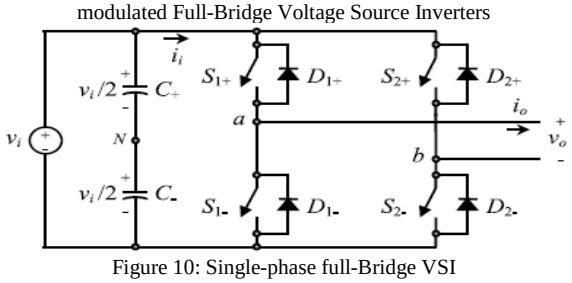

Figure 10: Single-phase full-Bridge VSI

Figure 10 represents the power procedure of a Full-Bridge VSI. This inverter is analogous to the Half-Bridge inverter; On the other hand, a following leg gives the neutral point to the load. As estimated that, together switches S_{1+} and S_{1-} (or S_{2+} and S_{2-}) cannot be on at the same time since a short circuit transversely the dc link voltage source v_i would be formed. There are four distinct (states 1, state 2, state 3, and state 4) and single indeterminate (state 5) switch states as represented in Table 2.

The indeterminate situation should be avoided so as to be for all time proficient of significant the ac output voltage. In order to avoid the short circuit transversely the dc bus and the indeterminate ac output voltage situation, the modulating procedure should make sure that whichever the peak or the base switch of each and every leg is on at any moment. It can be observed that the ac output voltage can obtain values up to the dc link value v_i , which is double that got with Half-Bridge VSI methodology. More than a few modulating procedures have been produced that are relevant to Full-Bridge VSIs.

Table 2 Switch states for a Full-Bridge single-phase VSI

State	State	v_a	v_b	v	Components Conducting
$_{1+}$ and $_{2-}$ are on and $_{1-}$ and $_{2+}$ are off	1	$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$ if >0
					$_{1+}$ and $_{2-}$ if <0
$_{1-}$ and $_{2+}$ are on and $_{1+}$ and $_{2-}$ are off	2	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$ if >0
					$_{1-}$ and $_{2+}$ if <0
$_{1+}$ and $_{2+}$ are on and $_{1-}$ and $_{2-}$ are off	3	$v/2$	$v/2$	0	$_{1+}$ and $_{2+}$ if >0
					$_{1+}$ and $_{2+}$ if <0
$_{1-}$ and $_{2-}$ are on and $_{1+}$ and $_{2+}$ are off	4	$-v/2$	$-v/2$	0	$_{1-}$ and $_{2-}$ if >0
					$_{1-}$ and $_{2-}$ if <0
$_{1-}$ $_{2-}$ $_{1+}$ and $_{2+}$ are all off	5	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$ if >0
		$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$ if <0

B. Selective Harmonic Elimination

Figure 11 and figure 12 represents a particular condition where only the essential ac output voltage is managed. This is identified as output managed by voltage termination, which derives from the fact that its implementation is without difficulty achievable by utilizing two phase-shifted square-wave switching signals.

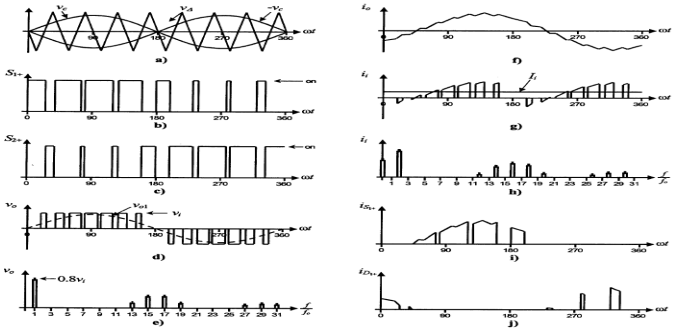

Figure 11: The Full-Bridge VSI. Ideal waveforms for the unipolar SPWM

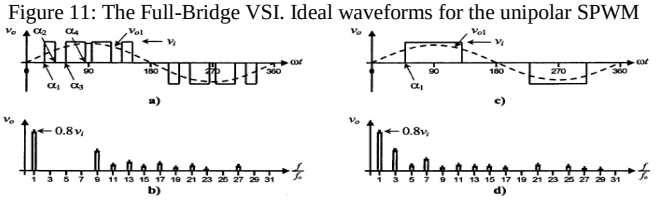

Figure 12: The Half-Bridge VSI. Ideal waveforms for the SHE procedure

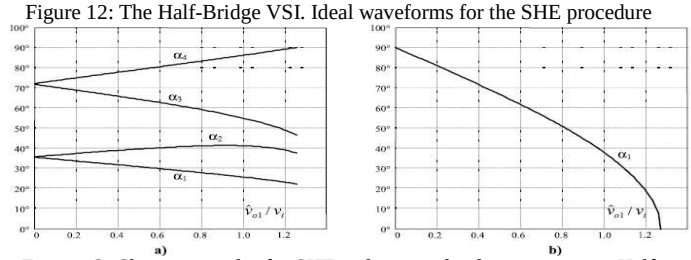

Figure 13: Chopping angles for SHE and essential voltage manage in Half Bridge VSIs: (a) essential manage and third, fifth, and seventh harmonic elimination; (b) essential control.

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Consequently, the magnitude of the essential factor and harmonics in the ac output voltage are specified by

$$\hat{v}_{oh} = \frac{4}{\pi} v_i \frac{1}{h} \cos(h\alpha_1), \qquad h = 1, 3, 5, \ldots$$

It can also be proved that for $\alpha_1 = 0$ square wave process is accomplished. In this case, the essential an output voltage is specified by

$$\hat{v}_{o1} = \frac{4}{\pi} v_i$$

Where the essential load voltage can be managed by the corrections of the dc link voltage.

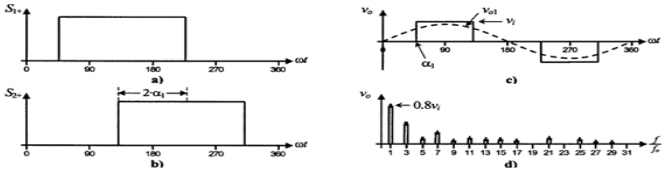
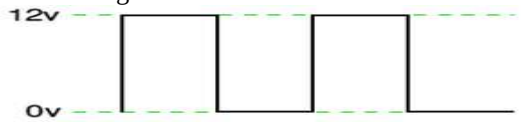


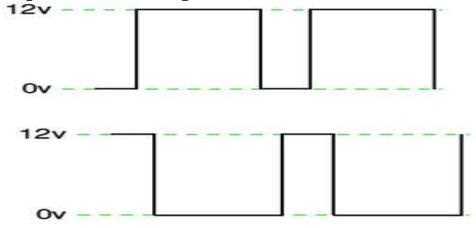
Figure 14: The Full-Bridge VSI. Perfect waveforms for the output manage by voltage termination

VII. Pulse Width Modulation (PWM)

Pulse Width Modulation (PWM) is the very important successful resources to accomplish steady voltage battery charging by switching the solar system controller's power modules. When in PWM instruction, the current from the solar arrangement tapers according to the battery's situation and recharging requires. Let us consider a waveform such as this: it is a voltage switching lies in between 0 V and 12 V. It is practically understandable that, because of the voltage is at 12 V for accurately as long as it is at 0 V, after that a 'appropriate apparatus' associated to its output will observe that the standard voltage and imagine it is being fed 6 V - accurately half of 12 V. So by changeable the width of the positive pulse - we can diverge the 'average' voltage represents in figure 15 below.



Likewise, if the switches maintain the voltage at 12 V for 3 times as long as at 0 V, the typical will be 3/4 of 12 V or 9 V, as represented below and if the output pulse of 12 V lasts not more than 25% of the on the whole time, after that the standard is represented in figure 16 below.



A. Pulse Width Modulator

Consequently, how accomplish we produce a PWM waveform? It's in reality extremely simple; first we produce a triangle waveform as represented in the diagram below. We contrast this with a d. c voltage, which we regulate to manage the relation of on to off time that we need. Whenever, the triangle is on top of the 'demand' voltage, the output goes high. Whenever the triangle is underneath the demand voltage, the output goes low.

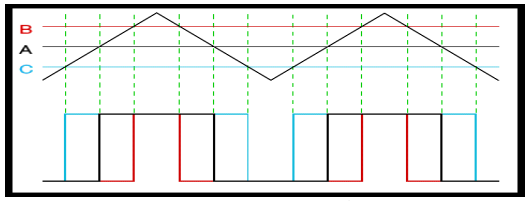
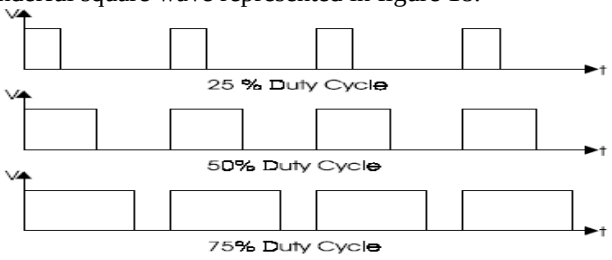


Figure 17: PWM Waveform

The triangle waveform, which has about equivalent ascend and descend slopes, is one of the commonest utilized, but we can utilize a saw tooth (where the voltage falls quickly and rinses slowly). We could utilize additional waveforms and the accurate linearity (how good the rise and fall are) is not excessively significant.

A supplementary resourceful performance applies Pulse Width Modulation (PWM) to generate the steady current through the coil. A PWM signal is not steady somewhat, the signal is on for fraction of its phase, and off for the rest. The duty cycle, D, represented to the percentage of the period for which the signal is on. The duty cycle can be everyplace from 0, the signal is for all time off, to 1, and where the signal is continuously on. A 50% duty cycle, D consequences in a wonderful square wave represented in figure 18.



B. PI Controller

The schematic block diagram of the PI speed controller is represented in Figure 19.

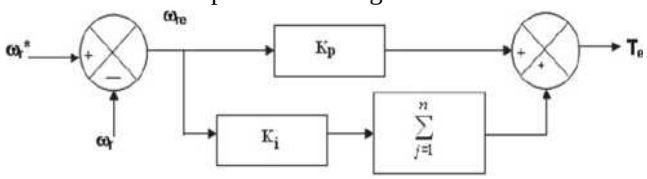


Figure 19: Schematic Block Diagram of PI Speed Controller

The output of the speed controller (torque command) at m^{th} moment is represented as below:

$T_e(m) = T_e(m-1) + K_p\_\omega_{re}(m) + K_i\omega_{re}(m)$

Wherever $T_e(m)$ is the torque output of the controller at the m^{th} moment, and K_p and K_i the Proportional and Integral gain constants, respectively.

A maximum value of the torque control is represented as,

$$T_{e(n+1)} = \begin{cases} T_{emax} & \text{for } T_{e(n+1)} \geq T_{emax} \\ -T_{emax} & \text{for } T_{e(n+1)} \leq -T_{emax} \end{cases}$$

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VIII. Modeling of Case Study

A. DSSC Fundamental Theory

DSSC theory has been started based on FACTS components, which is in fact a representation of a SSSC however in a slighter size, at a lesser charge, and with a advanced capacity. The circulated approach of the DSSC gives up further protection and enhanced controllability of power system.

Figure 20 represents an imaginary representation of DSSC utilized in a power system so as to control the power flow by altering the line impedance. Every one DSSC component is rated at about 10 KVA and is fasten in the region of the procession. The independently scheming of every one component furnishes an occasion to augment or diminish the impedance of the line or to depart it unaffected. By means of a great amount of components acting collectively, it will be sufficient to give up considerable power on the on the whole power flow in the line.

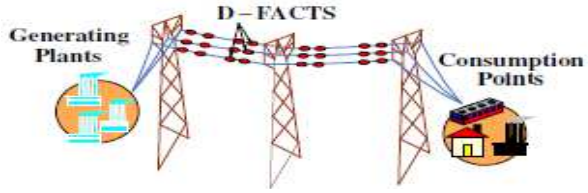

Figure 20: D-FACTS Deployed On Power Line

A DSSC component as represented in Figure 21, is self-possessed of a little rated (10 KVA) Single Phase Inverter (SPI) and a Single Turn Transformer (STT) with its connected controls, power supply circuits and incorporated communications capacity. The Single Turn Transformer STT is a significant module of the DSSC. It executes the utilization of the transmission conductor as a less important winding and is considered with elevated turn ratio which decreases the current manage by the inverter; consequently it will be achievable to utilize profitable IGBTs to appreciate lesser charge. The transformer core is fabricated of two parts that can be actually fastened just about the transmission line to represent a entire magnetic circuit.

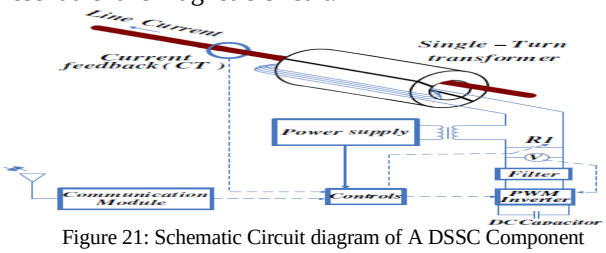

Figure 21: Schematic Circuit diagram of A DSSC Component

B. DSSC Impact on Power Flow

As represented before, DSSC is associated in sequence to the transmission line and thus has the capability of introducing a synchronous essential voltage that is in quadrature with the line current straight into the transmission conductor. As a consequence, the transmitted power turns a parametric purpose of the introduces voltage and can be confirmed as the consequence:

$$P_{12}=\frac{V_1 V_2}{X_L}\sin\delta-\frac{V_1 V_q}{X_L}\cos\left(\frac{\delta}{2}\right)\left[\frac{\sin\left(\frac{\delta}{2}\right)}{\sqrt{\left(\frac{V_1+V_2}{2V_2}\right)^2-\frac{V_1}{V_2}\cos^2\left(\frac{\delta}{2}\right)}}\right]$$

Where:

V_1 and V_2 = the bus voltage amplitudes;

V_q = the sequence introduces voltage amplitude;

δ= the voltage phase difference; and

X_L = the impedance of the line, assumed to be entirely inductive.

The DSSC can basically augment the communicable power as well as diminish it by reversing the divergence of the introduced ac voltage. This is significance noting that this characteristic is answerable for sustain the DSSC significant capability for power flow control in the entire system.

The distinction of the transmitted power verses load angle with dissimilar quadrate voltage introductions, for equivalent bus voltage amplitudes is represented in Figure 22.

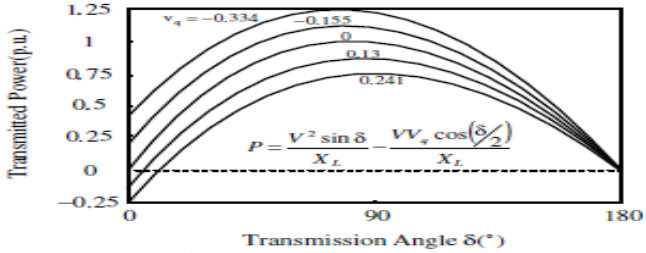

Figure 22: Variation of Transmitted Power by Quadrate Voltage Introduction

C. Reproduction Model Extracted For DSSC

The inverters which are straightly controlled impose additional complexity and elevated charge to be applied examine to indirectly controlled inverters, in addition their purpose is naturally interconnected with several punishment in terms of augmented losses, better circuit complexity and increased harmonic components in the output. As a consequence, the control method utilized for the DSSC representation investigated in this paper is based on indirect control method.

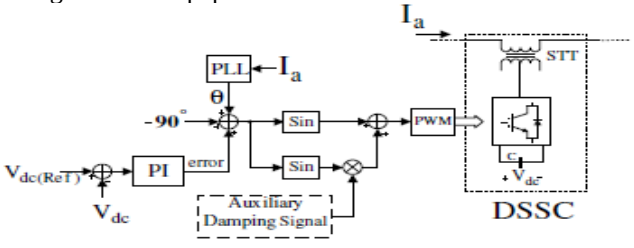

Figure 23: DSSC Control System and SPWM Generator

Figure 23 represents the DSSC control system and SPWM generator. The controller most important purpose is to embrace the charge constant on the dc capacitor and in addition to introduce a voltage that is in quadrature with the line current. A miniature phase displacement specifically, error, further than the necessary 90° between the introduced voltage and the line current is required to fix the dc capacitor voltage. The signal getting by analyzing V_{dc} with $V_{dc\ (ref)}$ is

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accepted through a Proportional Integral (PI) controller which produces the mandatory phase angle displacement or error. The Phase-Locked Loop (PLL) generates the fundamental synchronization signal, θ, which is the phase angle of the line current.

D. Transient Stability Improvement with DSSC

DSSC would improve the transient stability by fractional eliminating of the series impedance of the transmission line. The transient stability on the other hand, can be additional augmented by momentarily varying the compensation with a additional controller joined to the major control loop of DSSCs. For the period of the first acceleration stage of the machine, the controller increases the transmitted power by introducing advanced series voltage. Likewise, the deceleration of the machine is augmented basically by growing the line impedance and thus, declining the transmitted power. Figure 24 represented the power system measured as the case study in the following simulations.

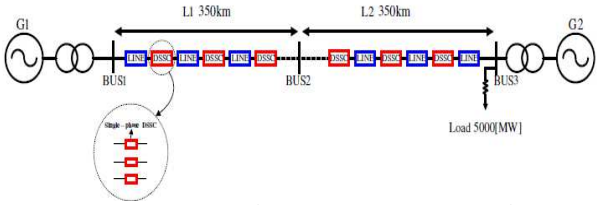

Figure 24: Simulation model of two-machine power system for transient stability study with DSSCs

With respect to Figure 24, it can be cleared that the load center is modeled by a 5000 MW resistive load. The load is fed by a local generation of 4000 MW (machine G2) and a remote 1000 MW plant (machine G1) which is associated to the load center through a long 500 KV, 700 km transmission line. The system has been originated so that the line transmits 950 MW which is close to its surge impedance loading (SIL=977 MW). $V_{dc\ (ref)}$ for each DSSC component is fixed at 2 KV, magnitude modulation percentage is set at 0.5, and the turn's ratio of STT is 1:100. Accordingly, by applying these adjustments, the introduced voltage of every one DSSC component is predictable to achieve a crest to crest value of 10 V. Concerning that the introduced voltage of each DSSC is 10 V, with the examination of achieving 4% compensation on transmission line, near 1400 DSSC components are mandatory in every one phase of the line. Figure 24 represents a superior illustration of DSSCs location in the transmission lines.

$$X_L = 230\Omega, X_{inj} = -9.5\Omega$$

$$\frac{X_{inj}}{X_L} \times 100 = \%Compensation$$

The negative sign for X_{inj} represents the capacitive mode of DSSCs to series compensation of the line.

In order to estimate the DSSC impact in the transient stability improvement, three different case studies are considered. The subsequently segment would present the whole simulation results for these states.

IX. MATLAB Design Of Case Study And Results

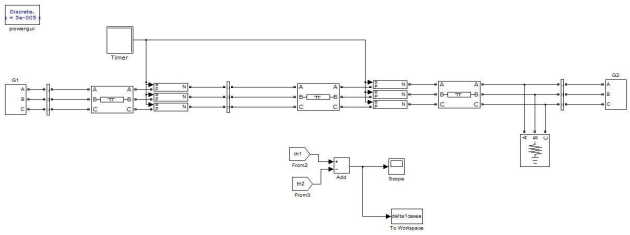

Figure 25: Simulation Model of Two-machine Power System for Transient Stability Study with DSSCs

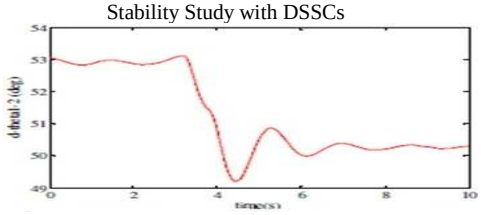

Figure 26: The Rotor Angle Difference Variation after the Fault with DSSCs

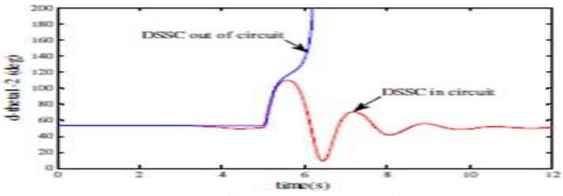

Figure 27: The Rotor Angle Difference Variation after the Fault without DSSCs and With DSSCs

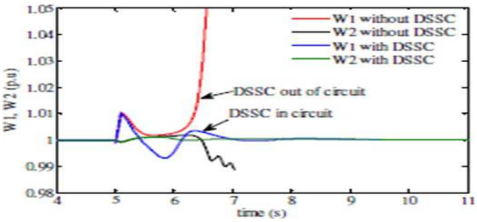

Figure 28: Variation of the Machines Angular Speed after the Fault without DSSCs and With DSSCs

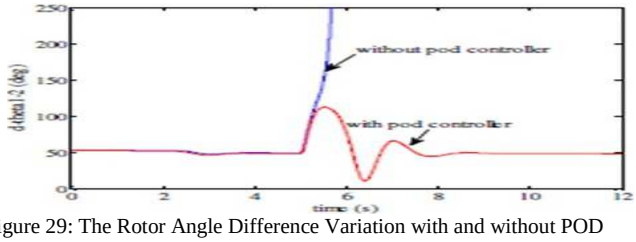

Figure 29: The Rotor Angle Difference Variation with and without POD

X. Conclusion

The enlargement of D-FACTS components has been announced as an effective approach to overcome the elevated charge accomplishment of FACTS relations. The circulated components are as well suitable to achieve some other auxiliary works such as transient stability improvement, power oscillation damping, etc. This learning served an examination of graphical-based simulation model for the DSSC which is in fact a lesser equivalent of SSSC. A two-machine power system is put under examination in order to verify the DSSC capacity for growing the transient stability of the whole system.

Simulation results demonstrate that when the DSSCs are out of service, the rotor angle between the machines, but when the

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DSSCs are in circuit, they steady the system still without a specific controller. In the after that, a rigorous fault is taken to occur in the system. It is shown that for this case, the system even with DSSCs in service becomes totally unstable. Hence, a POD controller is additional to the main control loop of DSSC for improving the transient stability margin of the system. Simulation results exhibit that in this case the system will remain stable after the fault removal. Consequently, the ability of distributed devices such as DSSC in the enhancement of the power system operation is certified.

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